CISTER – Research Centre in
Real-Time & Embedded Computing Systems

Quinquennium Report

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Aim and External Advisory Board

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This report provides a comprehensive overview of the activities and achievements carried out by the CISTER research unit during the quinquennium 2013-2017. It also provides an outlook for the future.

This report has been elaborated in collaboration with the CISTER External Advisory Board (EAB), which is composed by the following distinguished academics and representatives from the industry.

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Brief History

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The Research Centre in Real-Time and Embedded Computing Systems (CISTER) is based upon a research group created in 1997 at the School of Engineering (ISEP) of the Polytechnic Institute of Porto (IPP). Since then, it has grown to become one of the leading international research centres in real-time and embedded computing systems.

CISTER went through three previous international evaluation processes. In both the 2003 and 2007 evaluation processes, CISTER was granted the classification of “Excellent” (the highest possible mark at that time), being the only Portuguese unit in the areas of Electrical Engineering, and Computer Science and Engineering to top-rank in both evaluations. In 2013 CISTER went through another international evaluation process. It was an unfortunate process, with mistakes that led to achieving a lower ranking than what would be expected. The process lasted more than 3 years (it ended January 2017) and CISTER was evaluated only with “Very Good”.

In 2012, CISTER joined INESC-TEC as an associated autonomous research unit. However, the concept of association of research units (individually evaluated) was not considered in the 2013 evaluation process. Nonetheless, CISTER maintained the liaison with INESC-TEC during the quinquennium (2013-2017), with INESC-TEC being a secondary management institution (ISEP was the main management institution). For the current evaluation, which will institutionally frame CISTER for the quinquennium 2018-2022, ISEP will be the main management institution and the Faculty of Engineering of the University of Porto (FEUP) will be the secondary management institution. This comes as a natural evolution as CISTER includes researchers affiliated with ISEP (the majority) and FEUP since 2013. This also better reflects the long existing collaborations of CISTER with both ISEP and FEUP, given that FEUP is the academic institution that hosts most of the doctoral programs (e.g., the ECE or the dual-degree FEUP-CMU ECE programs) in which CISTER researchers are involved.

Finally, as Associate Labs will be considered by FCT in the future, and independently of the evaluation exercises, CISTER will assess the opportunities of associating with other research units (notably INESC-TEC) if strategic fit exists.

New Facilities

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Since 2012, CISTER is housed in a 3-storey autonomous building, entirely used by CISTER members and CISTER-related activities. The CISTER building is situated across the street from the ISEP campus and is also at a walking distance from the FEUP campus.

The building has over 1500 square-meters of area, out of which over 950 square-meters for offices, open-spaces, meeting rooms, hands-on labs and auditorium. In the past two years, CISTER accommodated around 70 people simultaneously on average. From 2012 until 2016, the use of the CISTER building required a significant financial effort from CISTER and ISEP, as the building was rented and a number of adaptations to enable its proper usage by CISTER were required. In 2016, the building was acquired by the Polytechnic of Porto and therefore that financial overhead (roughly 800 K Euros for the 5 years) was almost eliminated. Consequently, with the end of this financial constraint, in 2016, CISTER established a strategy of gradually growing its pool of researcher members to a target number of around 100. This strategy is currently being implemented with a special focus on targeting 30-35 active PhD students as well as around 10 research engineers (in support of the implementation and validation tasks related to R&D projects).

The CISTER building is organised into three main areas. The third floor is dedicated to housing management activities, including the offices for the research leaders, management, administrative personnel and senior faculty as well as two meeting rooms for support. The second floor is essentially used to host fundamental research activities (full-time research PhD members and PhD-students). Besides a number of offices and open-spaces to accommodate these full-time researchers, this floor has a kitchen, the main cafeteria and the general secretariat services. Additionally, it has two meeting rooms (with telco facilities) and a prayer room. Finally, the first floor is essentially used to accommodate industry-related research projects development, undergrad projects and outreach. In addition to the offices and open-spaces, in that floor, there is an auditorium and large hands-on labs which in conjunction are successfully used to host workshops, seminars and relatively large project events.

Taking advantages of the conditions offered by the new facilities, CISTER organized a number of industry-oriented workshops (the CiWork series - details provided later in the section “Tech Transfer and Outreach”), housed the CiTech initiative (a CISTER-driven Portuguese ecosystem for critical computing systems - details provided later in the Section “Tech Transfer and Outreach”), has already been responsible for more than 20 collaborations with more than 30 Portuguese companies, and hosted over 20 large meetings related to international projects.

Key People

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Currently, CISTER has 22 PhD members, 16 of which are integrated, and the remainder are collaborators. Integrated members have a stronger bond to the research unit, particularly in what concerns the commitment to contribute to CISTER scientific metrics. Among the 6 collaborator members, two focus essentially on management of science and technology and on industry outreach, namely Raghuraman Rangarajan (India) and Paulo Gandra Sousa, two devote less than 20% to research activities, namely Luis Nogueira and Paulo Baltarejo Sousa and two are recent Postdocs, namely Kai Li (China) and Kostiantyn Berezovskyi (Ukraine).

The current 16 integrated PhD members are: Anis Koubaa (Tunisia); David Pereira; Eduardo Tovar; Filipe Pacheco Paulo; Geoffrey Nelissen (Belgium); Konstantinos Bletsas (Greece); Luis Almeida; Luis Ferreira; Luis Miguel Pinho; Michele Albano (Italy); Muhammad Ali Awan (Pakistan); Patrick Meumeu Yomsi (Cameroon); Pedro Souto; Ramiro Sámano Robles (Mexico); Ricardo Severino and Vincent Nelis (Belgium).

The three core members for the application 2018-2022 are Eduardo Tovar, Luis Almeida and Luis Miguel Pinho.

All the other 13 integrated PhD members have relevant scientific activities during the quinquennium 2013-2017, as detailed in other sections of this report.

During the quinquennium 2013-2017, CISTER counted with other PhD integrated members that are not currently at CISTER but who developed relevant contributions. Namely, Mário Alves, Nuno Pereira and Stefan Petters (Germany), were integrated members in 2013 and 2014, Kjell Benny Åkesson (Sweden) was integrated member in 2015 and 2016, and Sana Ullah (Pakistan) was integrated member in 2014 and 2015. All these members were involved less than 50% per year, except for Stefan Petters (100% in 2013) and Sana Ullah (70% in 2014).

Other PhD members also enrolled activities of the research unit during the quinquennium but either for very short duration or recently graduated at CISTER, thus not being considered integrated members, namely Christos E. Chrysoulas (Greece), Maria Serna (Spain), Dorin Maxim (Romania), Gurulingesh Raravi (India), Borislav Nikolic (Serbia) and Ismael Carrión (Spain).

Below we report the evolution of the number of integrated PhD members during quinquennium 2013-2017. Many of the integrated PhD members are also professors; in terms of research, they typically account for 0.5 FTE (Full Time Equivalent). These include: Anis Koubaa; Eduardo Tovar; Filipe Pacheco Paulo; Luis Almeida; Luis Ferreira; Luis Miguel Pinho; and Pedro Souto. Note that both Anis Koubaa and Pedro Souto are accounted as 0.3 FTE in average. Eduardo Tovar is accounted as 0.3 in research and 0.2 in management of R&D. Filipe Pacheco is accounted as 0.5 in management of R&D.

Most of the other integrated PhD members are accounted as 1.0 FTE per year. Exceptions are Ricardo Severino and David Pereira who are 0.5 in research and 0.5 in management of R&D.

The number of Integrated FTE PhD members of CISTER has evolved as indicated in Table 1 during the quinquennium 2013-2017.

Table 1 – Integrated PhD Members (FTE)

	2013	2014	2015	2016	2017
Research	8.9	9.1	9.1	11.0	9.8
Management	1.0	1.2	1.2	1.7	1.7
TOTAL	9.9	10.3	10.3	12.7	11.5

During the quinquennium, the average FTE of integrated PhD members dedicated to research was 9.6. Table 2 shows how the average FTE of integrated PhD members evolved in the last three quinquennia.

Table 2 – Average Integrated FTE PhD Members for the Last Three Quinquennia

	2003-2007	2008-2012	2013-2017
Research	2.9	7.3	9.6
Management	0.1	0.9	1.3
TOTAL	3.0	8.2	10.9

Throughout the rest of this report, we will use FTE to refer to the average (in each specific quinquennium) FTE of integrated PhD members dedicated to research.

Relevance of the Focus Area

https://www.cister.isep.ipp.pt/research

Real-time computing systems are those in which the correctness depends not only on the logical result but also on the time at which the result is produced. These systems typically execute on embedded processors that represent around 96% of all processors available worldwide. Embedded processors are present in a wide variety of systems that operate in a growing number of sectors of the society.

Terms such as “cyber-physical systems” or “cooperating objects” have come to describe research and engineering efforts that tightly conjoin real-world physical processes and computing systems. The integration of physical processes and computing is not new; embedded computing systems have been in place for decades controlling physical processes. The revolution is steaming from the extensive networking of embedded computing devices and the holistic cyber-physical co-design that integrates sensing, computation, actuation, networking and physical processes.

Such systems pose many broad scientific and technical challenges, ranging from distributed programming paradigms to networking protocols, as well as systems theory that combines physical models and networked embedded systems. Notably, as the physical interactions imply that timing requirements are considered, real-time computing systems methodologies and technologies become pivotal in those systems. Moreover, many of these systems are often safety-critical, and therefore it is fundamental to guarantee other non-functional properties (such as safety, security or reliability) which often interplay among them and with timeliness requirements.

Real-time and embedded systems (RTES) are therefore a key strategic research, development and innovation area, pivotal to boosting the development of the future generation of highly complex and automated computing systems, which will be pervasive in virtually all application domains. Notable examples are aeronautics, aerospace and defence systems, robotics, autonomous transportation systems, Internet of Things, energy-aware and green computing, smart factory automation, smart grids or advanced medical devices and applications.

CISTER is focusing on research, development and innovation of RTES for 20 years. During these two decades, CISTER has established itself as one of the leading international research centres in the area, providing seminal results and achieving a high level of participation in many of the international R&D initiatives that drive the main developments of this class of systems.

International Leadership

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During the quinquennium 2013-2017, various CISTER researchers were elected to leading roles in relevant IEEE Societies or ACM Special Interest Groups. Notably, Eduardo Tovar is, since 2015, elected Vice-chair of the ACM SIGBED (Embedded Systems SIG; Chair is Insup Lee, University of Pennsylvania, USA). Luis Almeida is, since 2017, elected Vice-chair of the TC RTS (Technical Committee of Real-Time Systems of the IEEE Computer Society; Chair is Chenyang Lu, Washington University in St. Louis, USA). Luis Almeida ended in July 2016 an eight=year term as Trustee of RoboCup Federation, holding a Vice-presidency in 2011-2013. Luis Almeida was also Vice-Chair of EMSIG (EDAA Special Interest Group on Embedded Systems Design; Chair is Peter Marwedel, Dortmund University, Germany), from March 2012 to 2015.

During the quinquennium 2013-2017, various CISTER researchers were endorsed with leading roles in various key scientific events of the RTES area. These researchers include Eduardo Tovar, Luís Miguel Pinho, Luis Almeida, Luis Lino Ferreira, Vincent Nelis, Geoffrey Nelissen, Patrick Yomsi and Michele Albano, who are currently integrated researchers of CISTER.

In 2013, Eduardo Tovar was Program Chair of the 19th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS 2013), held in Philadelphia, USA, as part of the Cyber-Physical Systems Week (CPSWeek 2013); and was General Co-chair of the 8th IEEE International Symposium on Industrial Embedded Systems (SIES 2013), held in Porto, Portugal. Stefan Petters was Program Chair of the 25th Euromicro Conference on Real-Time Systems (ECRTS 2013), held in Paris. Mário Alves was Track Chair (Wireless Sensor Networks Track) in both the 34th IEEE Real-Time Systems Symposium (RTSS 2013), held in Vancouver, Canada, and the 35th IEEE Real-Time Systems Symposium (RTSS 2014), held in Rome, Italy. Luis Almeida was co-Chair of the 3rd and 4th RoboCup Workshop on Educational Robotics (WEROB 2013 and WEROB 2014), held in Conjunction with the RoboCup International Symposium. Anis Koubaa was the chair of Cooperative Robots and Sensor Networks (Robosense 2013) workshop in Ontario, Canada.

In 2014, Eduardo Tovar was General Chair of the 20th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS 2014), held in Berlin, Germany, as part of the Cyber-Physical Systems Week (CPSWeek 2014); Program Co-chair of the 27th GI/VDE-ITG International Conference on Architecture of Computing Systems (ARCS 2014) held in Lubeck, Germany; Program Co-chair of the 10th IEEE International Conference on Factory Communication Systems (WFCS 2014), held in Toulouse, France. Geoffrey Nelissen was Co-chair of the 8th Junior Researcher Workshop on Real-Time Computing (JRWRTC 2014), held in conjunction with the 22nd International Conference on Real-Time and Network Systems (RTNS 2014), in Versailles, France. Anis Koubaa was the chair of Cooperative Robots and Sensor Networks (Robosense 2014) workshop in Hasselt, Belgium. He is also appointed as an Associate Editor in Journal of Cyber-Physical Systems (Tailor & Francis).

Luis Miguel Pinho was General Co-chair and Patrick Yomsi was Posters Session Co-Chair of the 28th GI/VDE-ITG International Conference on Architecture of Computing Systems (ARCS 2015), held in Porto, Portugal. Nuno Pereira was the Program Co-chair and Eduardo Tovar was the General Chair of the 12th European Conference on Wireless Sensor Networks (EWSN 2015), held in Porto, Portugal. Also, Ricardo Severino was Program Co-chair of the Poster/Demo Session of the same conference (EWSN 2015). Luis Almeida was Program Co-Chair of the 8th International Workshop on Compositional Theory and Technology for Real-Time Embedded Systems (CRTS 2015) as well as Program Co-Chair of the RoboCup International Symposium and Program Co-Chair of the 15th IEEE International Conference on Autonomous Robot Systems and Competitions (ICARSC 2015).

In 2016, Luis Miguel Pinho was Program Co-Chair of the 21st International Conference on Reliable Software Technologies (Ada-Europe 2016), held in Pisa, Italy; and Program Co-chair of the 24th International Conference on Real-Time Networks and Systems (RTNS 2016). Vincent Nélis was WIP Chair of the 22th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS 2016), held in Vienna, Austria, as part of the Cyber-Physical Systems Week (CPSWeek 2016). Eduardo Tovar was Program Co-chair of the 22nd IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2016), held in Daegu, South Korea; and Program Co-chair of the ACM/IEEE 7th International Conference on Cyber-Physical Systems (ICCPS 2016) held in Vienna, Austria. Eduardo Tovar and Luis Almeida were Local Co-chairs of the 37th IEEE Real-Time Systems Symposium (RTSS 2016), held in Porto, Portugal. Geoffrey Nelissen was Program Co-Chair of the 9th International Workshop on Compositional Theory and Technology for Real-Time Embedded Systems (CRTS 2016), also Luis Lino Ferreira was program Co-chair of 4th IEEE International Workshop on Real-Time Computing and Distributed systems in Emerging Applications (REACTION 2016), both collocated with RTSS 2016. Anis Koubaa has been the Editor-in-Chief of the Robotics Software Engineering topic, in the International Journal of Advanced Robotic Systems (Sage Publishing).

In 2017, Patrick Yomsi was WIP Chair of the 29th EUROMICRO Conference on Real-Time Systems (ECRTS 2017), held in Dubrovnik, Croatia; and Special Sessions Co-Chair of the 12th IEEE International Symposium on Industrial Embedded Systems (SIES 2017), held in Toulouse, France. He is also an editorial board member of the International Journal of Advances in Systems and Measurements. Luis Lino Ferreira was Program Co-chair of the 13th IEEE International Conference on Factory Communication Systems (WFCS 2017), held in Trondheim, Norway. For the same conference WFCS 2017, Michele Albano was Co-Chair of the Special Session on “Pilots for Digital Factory Communication”, and Co-Chair of the Special Session “Emerging Technologies and Solutions for Smart Buildings” for the 22nd IEEE Conference on Emerging Technologies And Factory Automation (ETFA 2017), held in Limassol, Cyprus. Vincent Nelis was Program Co-chair of the 8th International Real-Time Scheduling Open Problems Seminar (RTSOPS 2017), held in Conjunction with ECRTS 2017, in Dubrovnik, Croatia. Luis Almeida was Program Co-chair of the 23rd IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2017), held in Hsinchu, Taiwan; Eduardo Tovar was General Co-chair of the ACM/IEEE 8th International Conference on Cyber-Physical Systems (ICCPS 2017), held in Pittsburgh, USA.

Internationalization

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CISTER is a truly international research centre. During the quinquennium 2013-2017 CISTER had, as full time researchers, individuals coming from more than 20 countries (Belgium, Brazil, Cameroon, Chile, China, Cuba, Egypt, Germany, Greece, India, Italy, Mexico, Nigeria, Pakistan, Portugal, Romania, Russia, Serbia, Spain, Sweden, Tunisia, Ukraine, etc.). CISTER researchers were participating in 17 international projects involving more than 200 international partners, both from academia and industry.

During the quinquennium 2013-2017, CISTER graduated 18 PhD students. From these graduates, 12 were foreigners coming from 9 different countries, including Cuba, Egypt, India, Iran, Mexico, Pakistan, Russia, Serbia and Ukraine. Many of the CISTER PhD graduates are now in prominent positions in either academia or industry, in Portugal or outside of Portugal. Concerning those that found positions outside of Portugal, we would like to mention the following: Vikram Gupta (2014), currently at Awidit Systems, India; Dakshina Dasari (2014), currently at Bosch Research, Germany; Gurulingesh Raravi (2014), currently at NVIDIA, Germany; José Marinho (2015), currently at ARM, UK; Borislav Nikolic (2015), currently at TU Braunschweig, Germany; Hossein Fotouhi (2015), currently at the Malardalen University, Sweden; Luis Oliveira (2016), currently at the University of Pittsburgh, USA; Artem Burmyakov (2016), currently at the Seoul National University, South Korea; or Maryam Vahabi (2016), currently at the Malardalen University, Sweden. These and other former CISTER researchers add to the already large network of CISTER's alumni in all continents.

During the quinquennium 2013-2017, CISTER researchers have published more than 300 scientific papers in renowned international conferences and peer-reviewed journals. Notably, around 60% of CISTER papers have external collaborations with academia (around 80% of the journal papers and 55% of conference papers). Out of those, 10% is with industry (2% of journal papers and 14% of the conference papers).

In the quinquennium, we can report relevant publications with colleagues from the following international academic institutions: Max-Planck Institute on Software Systems, Germany; University of York, UK; University of Amsterdam, The Netherlands; Université Libre de Bruxelles, Belgium; Lulea University of Technology, Sweden; Federal University of Rio Grande do Sul, Brazil; Barcelona Supercomputing Center, Spain; Politecnico Milano, Italy; Carnegie Mellon University, USA; TU Berlin, Germany; Federal University of Bahia, Brazil; Nagoya University, Japan; VTT, Finland; TU Eindhoven, The Netherlands; INRIA, France; ONERA, France; University of Modena and Reggio Emilia, Italy; Malardalen University, Sweden; Trinity College Dublin, Ireland; University of Pittsburgh, USA; University of Pisa, Italy; University of Padova, Italy; TU Delft, The Netherlands; Aalborg University, Denmark; Mondragon University, Spain; University of Cantabria, Spain; Federal University of Santa Catarina, Brazil; University of the Balearic Islands, Spain; University of the Basque Country, Spain; Hangzhou University, China; University of Lorraine, France; Lund

University, Sweden; University of Zaragoza, Spain; University of Waterloo, Canada; University of Macau, China, University of Sousse, Tunisia, King Fahd University of Petroleum and Materials, Saudi Arabia; Acadia University, Canada; University of Leeds, United Kingdom, CINVESTAV (centro de investigacion avanzada), México; University of San Luis Potosí, México, International Marrakech University, Morocco; Halmstad University, Sweden, Instituto Tecnológico de Informática, Spain, Technological University of Gdansk, Poland Cork Institute of Technology.

In the quinquennium, we can report important publications with colleagues from various international industrial partners: Thales, France; EADS (now Airbus), Germany; Honeywell, Czech Republic; GD, Canada; ATOS, Spain; Sysgo, Germany; AdaCore; Rapita Systems, UK; Bosch, Germany; AVL, Austria; Philips, The Netherlands; Schneider Electric, France; Gaitech Robotics, China; Virtual Infrastructure, Austria; AVL, Austria; INDRA, Spain; Philips, The Netherlands.

Besides the various chairing roles in multiple key scientific events during the period, most of the CISTER integrated PhD researchers were consistently involved in a large number of program committees as well. Table 3 gives a non-exhaustive overview only in the conferences we consider (see Section "Publications" later in this report) either core or top to CISTER.

Table 3 – TPC Membership of Core Conferences during the Quinquennium

	2013	2014	2015	2016	2017
RTSS	Koubaa	Koubaa	Almeida	Almeida Tovar Nélis	Almeida Bletsas Pinho Tovar Yomsi
ECRTS	Bletsas Pinho	Bletsas	Bletsas	Bletsas	Nélis Nelissen
RTAS	Almeida Nélis Pereira Tovar		Nélis Tovar	Bletsas Nélis	Almeida Nelissen Nélis
RTNS	Nélis	Nélis	Nélis	Nélis	Nelissen
RTCSA	Tovar, Almeida	Almeida, Tovar	Almeida Tovar	Almeida Awan Nelissen	Tovar Nelissen
ETFA	Almeida	Almeida	Almeida Bletsas Pinho Tovar	Almeida Tovar Pinho Bletsas	Albano Almeida Bletsas Pinho Nélis Tovar
WFCS	Not organized	Almeida Ferreira Koubaa	Almeida Ferreira Koubaa Tovar	Almeida Ferreira Koubaa Tovar	Albano Almeida Koubaa Tovar
SIES	Almeida Alves Pereira	Almeida Alves	Almeida Alves	Almeida Pinho	Yomsi Pinho
Ada-Europe	Pinho	Pinho	Pinho	Pinho	Pinho

During the quinquennium, CISTER hosted several international distinguished researchers within the CISTER Distinguished Seminar Series, including the following distinguished speakers: Prof. Giuseppe Lipari, Scuola Superiore Sant'Anna, Pisa, Italy (Feb 2013); Prof. George Lima, Federal University of Bahia, Bahia, Brasil (Mar 2013); Prof. Joël Goossens, Université Libre de Bruxelles, Brussels, Belgium (Mar 2013); Prof. Kees Goossens, Eindhoven University of Technology, Eindhoven, The Netherlands (Mar 2013); Dr. Orlando Moreira, ST-Ericsson, Eindhoven, The Netherlands (Apr 2013); Prof. Carlo Fischione, KTH Royal Institute of Technology, Stockholm, Sweden (May 2013); Prof. José Ramiro Martínez de Dios, University of Seville, Seville, Spain (Jul 2013); Prof. Leandro Soares Indrusiak, University of York, York, UK (Sep 2013); Prof. Sanjoy K. Baruah, Washington University, St. Louis, USA (Mar 2014); Prof. Radu Marculescu, Carnegie Mellon University, Pittsburgh, USA (Jul 2014); Prof. Frank Mueller, NC State University, North Carolina, USA (Sep 2014); Prof. Leandro Buss-Becker, Universidade Federal de Santa Catarina, Santa Catarina, Brasil (Jan 2016); Prof. J. Javier Gutiérrez, Universidad de Cantabria, Cantabria, Spain (Feb 2016); Dr. Daniel Gracia Perez, Thales, France (Apr 2016); Prof. Shinpei Kato, Nagoya University, Nagoya, Japan (Apr 2016); Prof. Enrico Bini, Università di Torino, Turin, Italy (Jul 2016); Dr. Mitra Nasri, Max Planck Institute for Software Systems, Kaiserslautern, Germany (May 2017); and Dr. Benny Åkesson, Embedded Systems Innovation by TNO, Eindhoven, The Netherlands (May 2017). Beyond the CISTER Distinguished Seminar Series, other seminars took place at FEUP, including Prof. Ubirajara Franco Moreno, Federal University of Santa Catarina (Jul 2013); Prof. Daniel Ferreira Coutinho, Federal University of Santa Catarina (Oct 2013); Dr. Martina Maggio, Lund University (Mar 2014); Prof. Iria Estevez Ayres, Carlos III University, Spain (Mar 2014); Prof. Alisson Brito, Federal University of Paraíba, Brazil (Oct 2014); Dr. Carlos Moreno, University of Waterloo, Canada (Feb 2017), Prof. Guilherme Bastos, Federal University of Itajubá, Brazil (Jun 2017).

There was also a considerable number of invited keynotes and invited talks given by CISTER researchers. Just to name a few, Eduardo Tovar was an invited speaker at the 13th International Workshop on Real-Time Networks (RTN 2014), held in conjunction with ECRTS 2014, in Madrid Spain. In 2017, Eduardo Tovar was a Keynote Speaker at the 7th Brazilian Symposium on Computing Systems Engineering (SBESC 2017), held in Curitiba, Brazil. Luis Almeida was an invited speaker at the 25th Anniversary of the Heinz Nixdorf Institut, Paderborn, Germany, in 2014. He also gave an invited talk at the French Summer School on Real-Time Systems (ETR 2015), Rennes, France and he was a keynote speaker at the Real-Time Networks Seminar (FNRS 2016), organized at ULB, Belgium, and at the 14th Latin-American Robotics Symposium (LARS 2017). In this period, Luis Almeida also gave numerous invited talks at research institutions such as ISAE in Toulouse, France, TUe in The Netherlands, University of Koblenz-Landau in Germany, Lund University, KTH, MDH and Linköping University in Sweden. Luis Lino Ferreira was an invited speaker at the 12th IEEE International Conference on Factory Communication Systems (WFCS 2016) Industry day, held in Aveiro, Portugal. Luis Miguel Pinho was an invited speaker in the 2013 Real-time Systems Symposium of the Spanish Informatics Congress.

In the 2013-2017 period, CISTER hosted a number of external PhD students: Andrea Baldovin, PhD Student in Computer Science at the University of Padua, Italy (Feb - Jul 2015), and Davide Compagnin, PhD student at the same university (Mar - Jul 2016); Fabrice Guet, PhD student at ONERA DTIM, Toulouse, France (Jul - Sep 2016); Matthias Becker, PhD student at Malardalen university, Sweden (Jul - Aug 2015 and Apr - Jul 2016); José Augusto Santos, PhD student at Federal University of Bahia, Brazil (Dec 2014 - Apr 2015); Fernando Gonçalves, PhD student at Federal University of Rio Grande do Sul, Brazil (Sep 2016 - Apr 2017); Aasem Ahmad, PhD student at the technical University Prague, Czech Republic (Mar - Jul 2017); Marcus Lindner, PhD student at Lulea University of Technology, Sweden (May 2016); Stefan Grösbrink, PhD student at Paderborn University (Jan - Feb 2013); Rafael Maestrelli, PhD student at Universidade Federal de Santa Catarina, Brazil, (Dec 2013 - Nov 2014); Daniel Ramos, PhD student at Universidade Federal de Santa Catarina, Brazil, (Jan - Sep 2015); Sidney Carvalho, PhD student at Universidade Federal

de Santa Catarina, Brazil, (Mar - Nov 2016); Moses Koledoye, PhD student at the University of Pavia in Italy (Feb - Apr 2017).

Last but not least, during the period CISTER hosted several established academics for short term stays. This naturally added to boosting further collaboration and resulting in several publications in relevant venues. Examples are Prof. Damien Masson from the Université Paris-Est, France (Jan - Jul 2015); Prof. Per Lindgren, from the Lulea University of Technology, Sweden (Apr-Jun 2015 and May - Aug 2016); Dr. Mitra Nasri, from Max Plank Institute on Software Systems, Germany (various periods during 2016 and 2017); Prof. Marisol García Valls, from Universidad Carlos III, Spain (Nov - Dez 2016); Prof. Ubirajara Franco Moreno, from the Federal University of Santa Catarina and Prof. Martina Maggio, Lund University, Sweden.

Publications

www.cister.isep.ipp.pt/docs

In the quinquennium 2013-2017, CISTER researchers have published around 100 international journal papers (out of which 85% in indexed journals with highly rated impact factors). Considering that CISTER had around 9.6 FTE integrated research PhD member per year during the quinquennium, this gives a healthy number of around 2 journal papers per year and per FTE integrated research PhD.

Naturally, the most common journal venue is the Real-Time Systems Journal (Springer), with 12 papers in this period. Various other papers were published in the ACM Transactions on Embedded Computing Systems (4 papers), IEEE Transactions on Industrial Informatics (4 papers) or the Elsevier Journal of Systems Architecture (5 papers). Other important journals where CISTER published in the period include the IEEE Transactions on Mobile Computing, IEEE Transactions on Computers, the ACM Transactions on Design Automation of Electronic Systems, the Springer Telecommunication Systems, the Elsevier Journal of Microprocessors and Microsystems, the Springer International Journal on Software Tools for Technology Transfer or the Elsevier Journal of Network and Computer Applications, Springer Journal on Soft Computing, IEEE Sensors Journal, IET Intelligent Transport Systems, International Journal of Advanced Robotic Systems, Information Sciences, Journal of Intelligent & Robotic Systems, Elsevier Computer Networks, IEEE Transactions on Wireless Communications.

Table 4 summarizes the main publication output of CISTER.

Table 4 – Publications during the Quinquennium

	2013	2014	2015	2016	2017	TOTAL
Books	2			1		**3**
Book Chapters	2	3	2	2	5	**14**
Book Editor		1		1	1	**3**
Journal papers (indexed)	6	17	24	21	15	**83**
Journal papers (non-indexed)	1	3	6	4	2	**16**
International Conference Papers	38	28	41	26	28	**161**
Workshop Papers	12	8	14	10	7	**51**
WiP/Demo/Poster papers	3	6	18	17	8	**52**

At the same time, CISTER researchers have heavily disseminated key results through presentations at the most prominent scientific meetings. CISTER systematically targets the top 3 conferences in real-time and embedded systems, namely the IEEE Real-Time Systems Symposium (RTSS), the Euromicro Conference on Real-Time Systems (ECRTS) and the IEEE Real-Time and Embedded Technology Applications Symposium (RTAS). These are tier-1 premier conferences typically with an acceptance rate in the range of 20-25%. Note that these papers are typically 10-12 IEEE format page-long. During the quinquennium, CISTER had 15 papers in these three conference series alone (see Table 5).

Table 5 – Publications in the 3 Top Core Conferences during the Quinquennium

	2013	2014	2015	2016	2017	TOTAL
RTSS	2				3	**5**
ECRTS			1	4	1	**6**
RTAS	1	1		1	1	**4**
TOTAL	**3**	**1**	**1**	**5**	**5**	**15**

Other core conferences in the area are: IEEE RTCSA (International Conference on Embedded and Real-Time Computing Systems and Applications); IEEE ETFA (Emerging Technologies in Factory Automation), specifically the Real-Time Networked Systems and the Factory Communications tracks); the IEEE WFCS (Conference on Factory Communication Systems); RTNS (Conference on Real-Time Networks and Systems); Ada-Europe (Conference on Reliable Software) and IEEE SIES (Symposium on Industrial Embedded Systems). Most of these are also very competitive conferences. In these 6 conference series, CISTER published 68 regular papers (16 papers in IEEE RTCSA; 15 in IEEE ETFA; 13 in RTNS; 9 in IEEE SIES; 8 in IEEE WFCS and 7 in Ada-Europe). See Table 6 for more details.

Table 6 – Publications in the other Core Conferences during Quinquennium

	2013	2014	2015	2016	2017	TOTAL
RTNS		4	4		1	**13**
RTCSA	6	4	2	2	2	**16**
ETFA	2	4	2	4	3	**15**
WFCS	n/a	1	3	2	2	**8**
SIES	4	2		3		**9**
Ada-Europe	1	2	3		1	**7**
TOTAL	**13**	**17**	**14**	**11**	**9**	**68**

Many other relevant conferences could be listed as venues for CISTER publications during the quinquennium; examples include: EDAA DATE; ACM EMSOFT; IEEE SECON; EWSN; IEEE CPSNA; Euromicro DSD; IEEE Globecom; Euromicro PDP; NASA Formal Methods Symposium.

Table 7 lists the aggregate number (per quinquennium) of CISTER main publication indicators for the last three quinquennia, while Chart 1 shows the trend per FTE, as defined previously; that is, average (in each specific quinquennium) FTE of integrated PhD members dedicated to research.

Table 7 – Main Publication Indicators for the Last Three Quinquennia

	2003-2007	2008-2012	2013-2017
Indexed Journal	6	24	83
Top Core Conference	4	14	15
Other Core Conference	16	14	68

While performance regarding publications in top conferences is maintained over the quinquennia, both the two other categories (other core conferences and indexed journal papers) have an important improvement in the quinquennium 2013-2017.

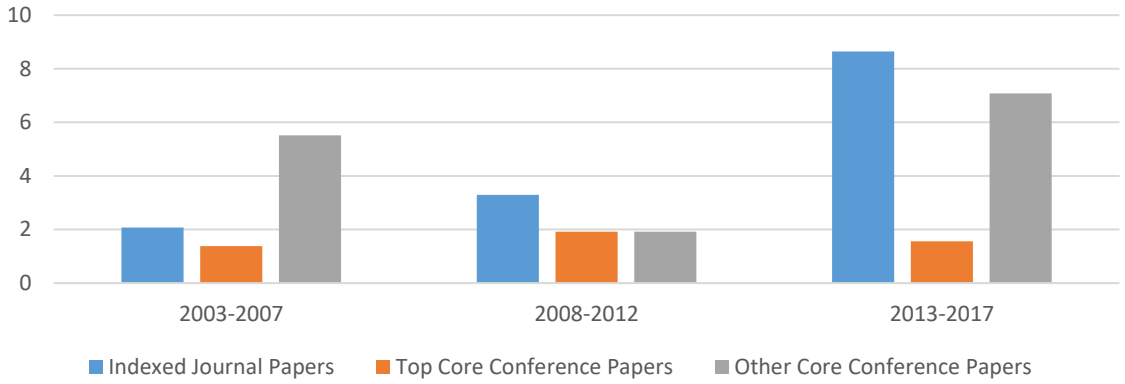

Chart 1 – Main Publication Indicators for the Last Three Quinquennia (per FTE)

CISTER researchers also enjoyed the opportunity they have had to explore other highly valuable roles and responsibilities. Various members of the unit co-authored and/or edited books. Some examples include "IoT Automation: Arrowhead Framework", edited in 2017 by CRC Press and co-authored by Luis Lino Ferreira and Michele Albano; the two volumes of the book "Robot Operating System (ROS)" edited by Anis Koubâa (the second volume being in the top 25% of the most downloaded eBooks in the relevant SpringerLink eBook Collection in 2016); the book "Memory Controllers for Mixed-Time-Criticality Systems: Architectures, Methodologies and Trade-offs" co-authored by Benny Åkesson; and the book "IEEE 802.15.4 and ZigBee as enabling technologies for low-power wireless systems with quality-of-service constraints" co-authored by Mário Alves, Nuno Pereira and Eduardo Tovar.

Moreover, CISTER researchers also edited special issues in relevant journals, such as in the Real-Time Systems Journal (2013 and 2017) and in the Journal of Intelligent and Robotic Systems (2016).

Finally, during the quinquennium, not only were CISTER researchers able to ensure a consistent participation and publication record in the best discussion forums of the area, their works were also nominated and granted awards that corroborate the high-quality of the research produced in CISTER. Overall, CISTER researchers won the "Outstanding Paper Award" in RTNS 2014 and in ECRTS 2016, and won "Best Paper Awards" in the Real-time Systems Track of RTCSA 2013, in GreenCom 2013 (4th IEEE Conference on Green Computing and Communications), in ESTIMedia 2015 (13th IEEE Symposium on Embedded Systems for Real-Time Multimedia), Ada Europe 2015, and RTNS 2017.

PhD Students Graduation

www.cister.isep.ipp.pt/phd

During the quinquennium 2013-2017, CISTER had around 24 PhD students active every year. Overall, 18 PhD students graduated and 17 new PhD students enrolled during the period. We expect that in cruise mode CISTER will have roughly 30-35 PhD students active every year, with an average of 4 to 5 PhD students graduating every year. Our impediment to grow from the 24 PhD students in 2013 was due to a combination of the following three factors: i) the new CISTER building drastically augmented our financial constraints (cost of use from 2012 to 2016); ii) the tuition fees for foreigners doubled in 2013; and iii) FCT individual PhD-student scholarships started to be more complex to obtain for non-EU citizens. As two of those facts disappeared in 2017 (tuition fee in FEUP is going to be halved starting in 2017/2018 and an exemption of the building usage cost took place in 2016), the expected target of having around 35 active PhD students every year is realistic and will be attained in a near future. To this end, we plan to enrol around 14 new PhD students already in 2017-2018.

CISTER PhD students (including visiting PhD students) are from multiple nationalities: Brazil; Chile; Cuba; Egypt; France; Germany; India; Iran; Italy; Mexico; Pakistan; Portugal; Dominican Republic; Russia; Serbia; Syria and Ukraine.

As it was already mentioned, most, if not all PhD graduates from CISTER are holding prominent positions in both academia and industry, in Portugal and abroad. CISTER PhD graduates from the quinquennium are nowadays at companies such as Bosch Research, NVIDIA or ARM or in prestigious academic institutions such as the Technical University of Braunschweig in Germany, the Malardalen University in Sweden, the University of Pittsburgh, USA or the Seoul National University in South Korea to name a few. CISTER is also glad to be able to retain as Postdocs some of its best PhD student graduates.

The PhD graduation committees of the CISTER PhD students are composed of typically 2 external members from reputed international institutions. In the period these included the following: Eindhoven University of Technology, The Netherlands; Lund University, Sweden; Lille University of Science and Technology, France; Scuola Superiore Sant'Anna Pisa, Italy; Nagoya University, Japan; Université Paul Sabatier, France; Federal University of Santa Catarina, Brazil; University of Luxembourg, Luxembourg; Technical University of Berlin, Germany; Linköpings Universitet, Sweden; Università di Modena e Reggio Emilia, Italy; Carnegie Mellon University, USA; Technische Universität Kaiserslautern, Germany; University of Pittsburgh, USA; Mälardalen University, Sweden; University of North Carolina at Chapel Hill, USA; University of York, UK; University of Catania, Italy; Universidad de Cantabria, Spain.

Table 8 lists the number of PhD students active in every year as well as the number of PhD students that graduated each year in the quinquennium 2013-2017.

Table 8 – PhD Student Indicators during the Quinquennium

	2013	2014	2015	2016	2017
Internal Students	24	26	24	21	20
External Students	2	1	6	3	3
Graduated Students	1	5	5	5	2
New enrolled internal students	2	4	3	2	5

Table 9 lists the average number of PhD students per year for the last three quinquennia and the number of PhD that graduated in each quinquennia, while Chart 2 shows the trend of those indicators per FTE, as defined previously; that is, average (in each specific quinquennium) FTE of integrated PhD members dedicated to research. It is worth noting that the number of active PhD students (per FTE) is steadily growing and is above 2 for the last quinquennium (more than 2 active students per FTE). It is also important to note that the number of graduated PhD students (per FTE) was multiplied by five in comparison to the previous quinquennium.

Table 9 – PhD Student Indicators for the Last Three Quinquennia

	2003-2007	2008-2012	2013-2017
Average Active Internal Students per Year	4	15	23
Number of Graduated Students per Quinquennium	2	3	18

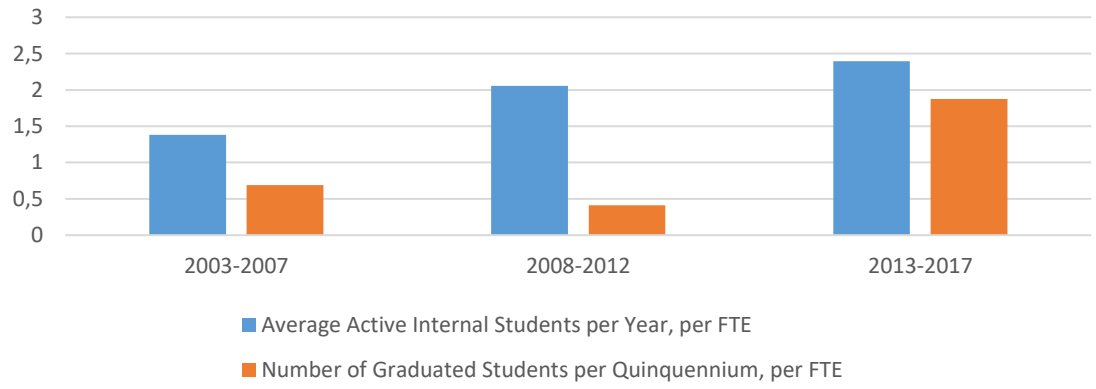

Chart 2 – PhD Student Indicators for the Last Three Quinquennia (per FTE)

Projects

www.cister.isep.ipp.pt/projects

During the evaluation period, CISTER was able to secure a continuous stream of fundamental and industry driven projects with a total funding of over € 3,500,000.00 (see details in Section "Funding", next), in the context of which CISTER researchers delivered excellent theoretical/foundational results and have also developed tools and prototypes with a strong potential for industrial exploitation. More details about these will be provided in the Section "Research Highlights".

Noteworthy is the fact that, from the total of projects active during the evaluation period, 14 are international industry-driven projects, in collaboration with many key industrial players such as Infineon, Airbus, Siemens, AVL, Thales, IBM, NXP, Magneti Marelli, Philips, Renault, Continental, Bosch, Schneider, Vestas, among many others.

Table 10 lists the number of active projects in each year, while Table 11 gives the average number of active projects per year within each quinquennium.

Table 10 – Active Projects during the Quinquennium

	2013	2014	2015	2016	2017
International Projects	7	7	8	9	11
National Projects (FCT + ANI)	13	12	9	2	2

Table 11 – Active Projects, Average per Year for the last three Quinquennia

	2003-2007	2008-2012	2013-2017
International Projects, Average per Year	1.0	2.8	8.4
National Projects, Average per Year	1.8	5.4	7.6

It is important to note that even if the number of national projects (typically FCT fundamental research projects) were decreasing steeply (as already mentioned, during the quinquennium FCT only opened a full-fledged call for proposals in 2014 and now in 2017, for which results are not yet known), the average number of active national projects was growing over the quinquennium

and also per FTE, as shown in Chart 3. Notably, the number of active international projects per FTE more than doubled when compared to previous two quinquennia.

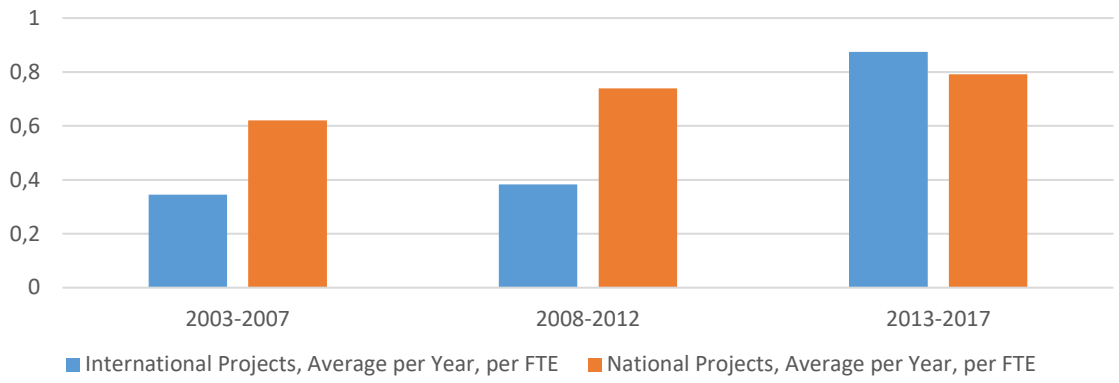

Chart 3 – Active Projects, Average per Year for the last three Quinquennia (per FTE)

CISTER was actively involved in several international projects touching different topics of RTES, and contributed with foundational work and innovative technology to support the associated use-cases, covering various application domains. Notably, CISTER researchers showed a sustained engagement with leading roles in these projects, either sharing use-case leadership with a distinguished industry partner, or with work package or project coordination. Just to mention a few, Robles was tech leader of DEWI and SCOTT; Pinho was P-SOCRATES coordinator; Severino is Work-Package Leader in SafeCOP and member of the project management team; Nelissen was core tech leader in CONCERTO and WP leader. In what follows, we briefly highlight a few of CISTER's contributions in the most relevant industry driven international projects, in which the research centre was involved.

Starting with P-Socrates, CISTER assumed the coordination and the technical management of this FP7 project, which aimed at tackling both performance and predictability on advanced embedded processors, by developing new techniques for exploiting the parallel capabilities of many-core embedded platforms in a predictable way. In addition, CISTER was leading the timing and schedulability analysis work package. The project output around 60 papers, 2 dozen with CISTER participation (with 2 best paper awards), and involved more than 5 PhD students (2 at CISTER). The exploitation plan included a post-project agreement for the continuing development of UpScale, now also in the scope of the Heterogeneity Alliance (heterogeneityalliance.eu). The focus on increased real-time performance of multi-core systems was pushed even forward in CONCERTO and EMC2, both ARTEMIS/FP7 projects.

CONCERTO aimed at delivering a reference multi-domain architectural framework for managing component-based non-functional requirements derived at design time, and preserved and monitored at run-time. Again, CISTER was the leader of a key work package that was focused in establishing the runtime monitoring solutions for the project. CISTER developed tools for schedulability and response time analysis for avionics systems and implemented a runtime monitoring and verification library for the ORK+ micro-kernel integrated in the GNAT cross-compiler for Leon 2/3.

In the EMC2 project (one of the largest ever ARTEMIS/FP7 projects approved), CISTER's focus was in the research-oriented work packages, mainly in two of the "Living Labs", leading a use case in automotive (together with Critical Software), and was involved in another use case in avionics (led by the Airbus Group). EMC2 aimed at providing the handling of mixed criticality applications under real-time conditions, scalability and utmost flexibility, full scale deployment and management of integrated tool chains, through the entire lifecycle.

The same engagement was ascertained in other ARTEMIS projects which instead focused in the communications perspective of RTES, in particular Cyber Physical Systems (CPS), such as in DEWI, one of the largest projects on embedded sensor wireless technology, in which CISTER played a core part by being selected to chair the technical board, as member of the strategic board, and as leader of the aeronautics domain. In addition, CISTER led the project's activities on standardization, regulation and certification. An important outcome of these activities was the effort on sensor networks standardization in ISO JTC1/WG7.

Similarly, the efforts in MANTIS and Arrowhead (ARTEMIS projects) also involved coordination roles from CISTER, in particular in MANTIS, whose objective was to provide a proactive maintenance service platform architecture based on CPS, CISTER researchers lead two work-packages, one related to dissemination and another related to the development and integration of sensors into industrial equipments. In Arrowhead, whose goal was to enable collaborative automation by networked embedded devices, CISTER led two tasks and was part of the Arrowhead Framework Coordination group (whose work continued after the end of the project). CISTER extended the publish/subscribe paradigm to SOA-supported QoS, and drove the research on QoS for distributed systems obeying the "cloud of clouds" design. In the follow-ups of these projects, CISTER maintains a distinguished role, particularly in Productive 4.0 and on new proposals.

In SCOTT, which focus on enabling efficient and trustworthy connectivity to support the ubiquity of intelligent embedded systems, CISTER is a member of the core team, accumulating the leadership of the reference architecture for the development of the infrastructure design guidelines; the co-leadership (together with Embraer) of the effort on aeronautics and the membership of the SCOTT Strategic Board, along with the project leader (Virtual-Vehicle) and 17 Large Enterprises (LEs).

CISTER also participates in the recently approved Productive 4.0 project, an ECSEL/H2020 lighthouse project, and one of the most important European initiatives in the ICT domain, whose goal is to strengthen the international leadership of European industry. CISTER involvement in this project will focus on the evolution of its QoS support for IoT applications, the reinforcement of a line of work coming from previous European projects such as Arrowhead and Mantis. Finally, two other complementary and recently approved ECSEL/H2020 projects, which also deserve a remark are ENABLE-S3 and SafeCOP.

ENABLE-S3 aims at substituting today's cost-intensive verification & validation efforts by more advanced and efficient methods to pave the way for the commercialization of highly automated CPS. CISTER is involved in three of the ENABLE-S3 use cases, namely: a Traffic Jam Pilot, co-led by CISTER and GMV Skysoft; a Touch and Go Assistant led by Airbus; and the smart and autonomous farming use case, led by TTControl. CISTER researchers is contributing to the safety and security aspects being tackled by the project, namely, static and dynamic formal verification, vehicle platooning, and real-time scheduling analysis.

On the other hand, SafeCOP focuses on safe and secure Cooperating CPS characterized by the use of wireless communication, multiple stakeholders and dynamic system definitions (openness) in unpredictable operating environments. CISTER has a leading role in one of the key work-packages which addresses safe and secure wireless communications, is a member of the project management team and is co-leading an automotive use-case together with GMV Skysoft.

Some additional details are listed next for these various international industry-driven projects that were active during the quinquennium 2013-2017. In the figures presented, funding is for CISTER only.

ARROWHEAD
Cooperative automation around the Internet of Things and Service Oriented Architectures.

207 k EUR - 03/2013 - 02/2017
77 Partners
Honeywell, ST Microelectronics, Schneider Electric, Fiat, Ford, Fagor, Airbus, etc.

CarCoDe
Platform for Smart Car - Car Content Delivery

58 k EUR - 07/2013 - 06/2015
13 Partners
Thales, NXP, Airbus, PT Inovação, etc.

CONCERTO
Component Assembly with Round Trip Analysis for Energy Efficient High-integrity Multi-core Systems

375 k EUR - 05/2013 - 04/2016
14 Partners
Airbus, Thales, Critical Software, etc.

DEWI
Dependable Embedded Wireless Infrastructure

390 k EUR - 03/2014 - 02/2017
55 Partners
Volvo, NXP, Airbus, Philips, Valeo, Critical Materials, ISA, GMV Skysoft, etc.

EMC²
Embedded multi-core systems for mixed criticality apps in dynamic and changeable RT environments

307 k EUR - 04/2014 - 03/2017
96 Partners
Thales Alenia Space, Freescale, Rockwell Collins, TomTom, Ericsson, Siemens, Philips, etc.

ENABLE-S3
European Initiative - Enable Validation for Highly Automated Safe and Secure Systems

296 k EUR - 05/2016 - 04/2019
67 Partners
Thales, TTTech, Siemens, Airbus Defence & Space, IBM, Renault, Toyota, etc.

ENCOURAGE
Embedded iNtelligent COntrols for bUildings with Renewable generAtion and storage

266 k EUR - 06/2011 - 11/2014
10 Partners
Atos, Energinord, Enel, ISA, etc.

ENERGAWARE
Energy Game for Awareness of energy efficiency in social housing communities

154 k EUR - 02/2015 - 01/2018
5 Partners
Plymouth University, UPC, EDF Energy, etc.

MANTIS
Cyber Physical System Based Proactive Collaborative Maintenance

281 k EUR - 05/2015 - 04/2018
47 Partners
Fraunhofer, Fagor, Philips, Adira, Atlas Copco, Continental, etc.

PRODUCTIVE 4.0
ICT for digital industry and optimized supply chain management

57 k EUR - 05/2017 - 04/20
108 Partners
Airbus Group, Thales, BMW, Volvo, NXP, Ericsson, SAP, Bosch, ABB, etc.

P-SOCRATES
Parallel SOftware framework for time-CRitical mAny-core sysTEmS

544 k EUR - 10/2013 - 12/2016
7 Partners
Barcelona Supercomputing Centre, Atos, ETH Zurich, etc

RECOMP
Reduced Certification Costs for Trusted Multi-core Platforms

456 k EUR - 04/2010 - 03/2013
39 Partners
Intel, Honeywell, Infineon, PSA Peugeot Citroën, Delphi, EADS, etc.

SAFECOP
Safe Cooperating Cyber-Physical Systems using Wireless Communication

300 k EUR - 04/2016 - 03/2019
26 Partners
Thales, GMV, Tekever, etc.

SCOTT
Secure COnnected Trustable Things

197 k EUR - 05/2017 - 04/20
56 Partners
Embraer, NXP Semiconductors, Nokia, Ericsson, Siemens, Bosch, etc.

In the quinquennium CISTER was coordinating (in AVIACC CISTER was only participant) the following FCT projects. The funding figures are CISTER only.

AVIACC
Analysis and Verification of Concurrent Critical Programs

24.1 k EUR - 05/2012 - 04/2015

MASQOTS
Mobility management in WSN under QoS constraints using COTS technologies

94.8 k EUR - 02/2011 - 06/2014

PATTERN
Programming abstractions for wireless sensor networks

149 k EUR - 06/2013 - 09/2015

REGAIN
Real-time scheduling on general purpose graphics processor units

139 k EUR - 04/2012 - 07/2015

REHEAT
Real-time scheduling on heterogeneous multicore architectures

130 k EUR - 02/2010 - 01/2013

REPOMUC
Real-time Power management on partitioned MultiCores

106 k EUR - 02/2011 - 01/2014

REWIN
Real-Time Guarantees in Wireless Sensor Networks

68 k EUR - 02/2010 - 01/2013

SENODS
Sustainable ENergy-Optimized Datacenters

219 k EUR - 10/2010 - 12/2013
Portugal Telecom, Carnegie Mellon, FEUP

SMARTS
Slack Management in Hierarchical Real-Time Systems

158 k EUR - 04/2012 - 09/2015

SMARTSKIN
Densely instrumented physical infrastructures

141 k EUR - 03/2012 - 02/2015
Critical Materials, Embraer

VIPCORE
Virtual Processor-based Multicore Scheduling

94.8 k EUR - 02/2011 - 06/2014

PATTERN
Programming abstractions for wireless sensor networks

149 k EUR - 06/2013 - 09/2015

REGAIN
Real-time scheduling on general purpose graphics processor units

139 k EUR - 04/2012 - 07/2015

REHEAT
Real-time scheduling on heterogeneous multicore architectures

111 k EUR - 02/2011 - 06/2014

In the quinquennium CISTER was involved in the following industry-driven national consortia (V-SIS, KHRONOSIM), Networks of Excellence (HiPEAC-3) and COST actions (TACLe).

TACLe
Timing Analysis at the Code Level.

11/2012 – 11/2016
20 partners

HIPEAC 3
European NoE on High Performance and Embedded Architecture and Compilation

3.8MEUR (global) - 01/2013 - 12/2015

KHRONOSIM
Control real-time physical and virtual systems

87.9 k EUR - 10/2016 - 09/2018
2 Partners
Critical Software, University of Coimbra

V-SIS
Sistema de Validação de Sistemas Críticos

53 k EUR - 01/2014 - 07/2015
2 Partners

Funding

www.cister.isep.ipp.pt

During quinquennium 2013-2017, CISTER was able to secure around 5.9 million euros of competitive funding (FCT pluriannual funding, project awards and direct funding from industry and services). The split between institutions is: 5.5 MEuros (ISEP) and 0.4 MEuros (FEUP). These are the values of income coming from external sources, except when stated otherwise, per year. Note that faculty members (Eduardo Tovar, Filipe Pacheco, Luis Miguel Pinho, Luis Almeida, Luis Lino Ferreira, Pedro Souto, etc.) are not accounted in this section.

Table 12 lists the income for the various types of competitive funding that CISTER received in the quinquennium.

Table 12 – Income from Competitive Funding (in euros) during the Quinquennium

	2013	2014	2015	2016	2017	TOTAL	TOTAL ISEP	TOTAL FEUP
FCT Funding (euros)	**681,193**	**1,032,843**	**647,484**	**701,259**	**641,000**	**3,703,779**	**3,508,500**	**195,279**
pluriannual funding	72,600	71,900	0	121,000	400,600	**666,100**	666,100	0
projects	194,893	403,643	299,784	27,159	0	**925,479**	784,200	141,279
co-funding of inter. projects	115,900	402,000	253,500	512,000	211,200	**1,494,600**	1,485,600	9,000
direct HR contracts	88,900	5,700	0	0	0	**94,600**	94,600	0
direct grants	208,900	149,600	94,200	41,100	29,200	**523,000**	478,000	45,000
EC Funding (euros)	**528,142**	**70,151**	**312,238**	**288,357**	**281,659**	**1,480,547**	**1,273,659**	**206,888**
projects	368,145	39,251	170,038	59,000	113,059	**749,493**	712,659	36,834
co-funding of inter. projects	159,997	30,900	142,200	229,357	168,600	**731,054**	561,000	170,054
Other Intern. Funding	**22,600**	**14,300**	**14,600**	**9,200**	**13,700**	**74,400**	**74,400**	**0**
Other National Funding	**34,100**	**133,300**	**328,000**	**58,700**	**20,600**	**574,700**	**574,700**	**0**
Direct Industry & Services	**7,200**	**3,500**	**20,000**	**0**	**39,600**	**70,300**	**70,300**	**0**
TOTAL	**1,273,235**	**1,254,094**	**1,322,322**	**1,057,516**	**996,559**	**5,903,726**	**5,501,559**	**402,167**

A few observations are to be made. There is a decline in FCT projects and FCT support of direct HR contracts and direct PhD-students grants. This is because the calls for these opportunities were very scarce in the period. Actually only one global (that is, without constraints of funding or PIs) FCT project call was completed during the quinquennium. Furthermore, the number of calls for PhD-student grants was reduced dramatically in the period and the requirements for non-EU students made more difficult the consideration of these students.

Notably, the overall pluriannual funding of the unit in the quinquennium accounts only for € 666,100.00 (11% of the overall competitive funding secured during the quinquennium). Competitive funding for international projects accounts for € 2,975,147.00 (over 50% of the overall funding). European Commission funding accounts for around 25% of the overall competitive funding, and represents twice the volume of the pluriannual funding. Direct industry income includes contracts such as with Portugal Telecom, EFACEC, Honeywell Europe or INOVA+.

Table 13 – Competitive Funding (in Euros) Indicators for the Last Three Quinquennia

	2003-2007	2008-2012	2013-2017
Overall	595,000	2,628,201	5,903,726
FCT Pluriannual	315,000	293,191	666,100
EC	260,000	313,633	1,480,547
International Projects	260,000	1,113,423	2,975,147
Direct Industry and Services	10,000	14,320	142,000

Chart 4 shows the trend of those funding indicators per FTE, as defined previously; that is, average (in each specific quinquennium) FTE of integrated PhD members dedicated to research. Note that values are for yearly average of funding, except for Direct Industry and Services, for which the value is for each quinquennium. The capability of attracting EC funding per FTE almost doubled when compared to the quinquennium 2003-2007 and almost quadrupled when compared to the quinquennium 2008-2012. Similar growth exists regarding international projects funding. The growth is much higher regarding the ability to attract direct industry funding, as a result of the strategy CISTER is implementing with the CiTech effort.

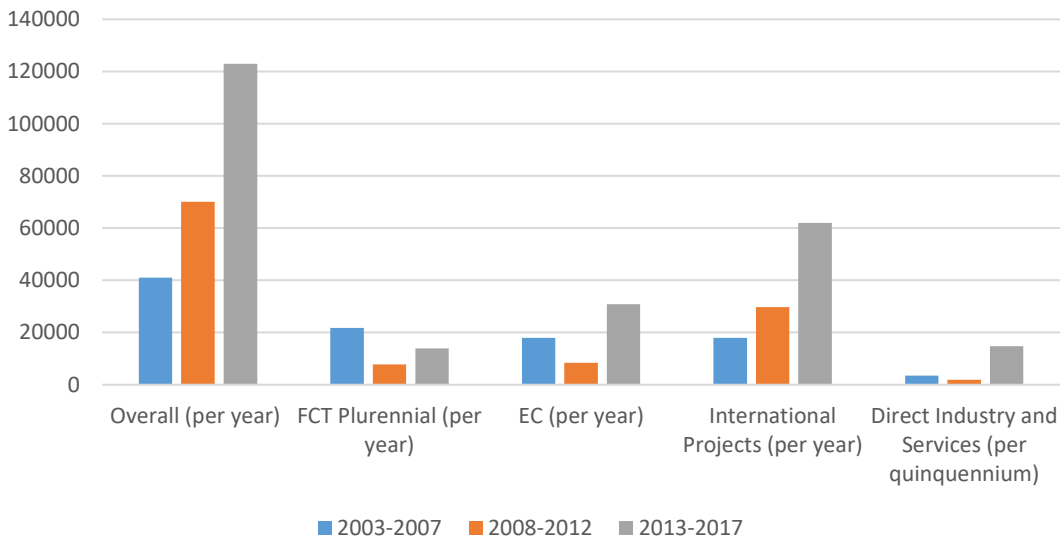

Chart 4 - Competitive Funding (in Euros) Indicators for the Last Three Quinquennia (per FTE)

Research Highlights

https://www.cister.isep.ipp.pt/research

Timing analysis for multicore systems

CISTER researchers have produced a wide range of contributions on the timing analysis of multicore platforms and more particularly on the impact that shared hardware resources such as interconnects and cache memories may have on the timing performances of real-time applications. Indeed, the underlying architecture of commercially available multicore platforms is extremely complex and non-amenable to straight-forward timing analysis due to hardware resources that are shared by cores and applications. With the increasing presence of multicore platforms in safety critical domains such as automotive, railway and avionics, there is a growing need for models that allow safe and reliable analyses of the timing properties of applications running on such platforms. Two PhD theses on this specific topic were conducted during the evaluation period (one was successfully defended in May 2014 and another started in 2015). This line of work led to 3 journal publications and 7 conference papers (among which 1 outstanding paper award at ECRTS16) during the quinquennium 2013-2017 (with 4 more publications outside of the evaluation period). Furthermore, CISTER researchers have been working on the development of software and hardware solutions to mitigate the impact of the shared hardware resources on the timing unpredictability of applications running on multicores, some of which were developed in direct collaboration with Bosch and Thales. Eight additional papers were published on this topic in peer-reviewed conferences and journals.

High-performance computing for RTES

Another example of the internationally relevant contributions of CISTER is the leadership of the European P-SOCRATES FP7 project, which addressed one of the most challenging topics in the real-time embedded domain: how to tackle both performance and predictability on advanced embedded processors. The project was a natural follow-up of CISTER leadership in the area, with research works in topics such as multicore timing analysis and parallel real-time scheduling, as well as in promoting meetings and workshops that brought together both the real-time and the high-performance computing (HPC) communities (in particular within HiPEAC). P-SOCRATES joined together a set of academic and industrial partners, from real-time and HPC, to develop new techniques for exploiting the parallel capabilities of many-core embedded platforms in a predictable way. Besides coordination and technical management, CISTER was also leading the timing and schedulability analysis work package. The project provided significant outputs in both research and technology. The project output around 60 papers, of which more than 2 dozen had CISTER participation (2 best paper awards for works led by CISTER [Ada-Europe 2015][RTNS17]), and more than 5 PhD students supported (2 at CISTER). Significantly, CISTER was the first to propose enriching a real-time parallel task model with control-flow information. The project also released a toolkit for the development of HPC real-time applications, the UpScale SDK

(www.upscale-sdk.com), which includes the UpScale Analyser, for timing and schedulability analysis of real-time parallel applications, developed at CISTER. The exploitation plan included a post-project agreement for continuing development of UpScale, now also in the scope of the Heterogeneity Alliance (heterogeneityalliance.eu). The visibility of the project is also attained by the project's industrial advisory board, which has grown from an initial set of 5 members to the final count of 13, including relevant companies such as Airbus D&S, Expert System, Airbus IG, Honeywell, SAAB and Bosch.

Self-suspending tasks

Since 2015, CISTER researchers have been working on the so-called self-suspending task model. This line of work studies the timing properties of common application features that require applications to momently suspend their execution to implement, for example, synchronisations barriers, to enforce the consistency of data shared by multiple actors, to access data saved on external storage devices, or to wait for data computed by GPUs, FPGAs or co-processors. In 2015, CISTER researchers unveiled major flaws in the published theory on self-suspending tasks. This discovery had a major impact in the real-time systems research community due to its importance (i.e., it invalidated results on single-,multi- and many-core processors, resources sharing, distributed systems, etc.) and its scale (i.e., more than 20 works published in renown conferences and journals and several results taught in textbooks were proven incorrect). CISTER researchers co-assembled an international team of experts (from Portugal, Germany, UK, USA, France, Spain and China) to scrutinise the validity of all published results on related topics. CISTER co-authored a technical report summarizing the results of that research [xx]. The work of CISTER did not end there though. Since mid-2015, researchers from CISTER have published 3 papers in major real-time systems conferences [ECRTS15][ECRTS16][SIES16] (totalling already 36 citations), and submitted 2 journal papers (already 27 citations of their technical report versions) to solve the issues detected in the state-of-the-art. Those results were promoted in two European projects (namely, Artemis project CONCERTO and CISTER-led FP7 project P-SOCRATES). Additionally, the CISTER discoveries on the analysis of self-suspending tasks motivated a collaboration with the Max-Planck Institute on Software Systems, Germany, to mechanically prove the validity of published timing analyses for real-time systems in general and self-suspending tasks in particular. The main goal of this collaboration is to improve the confidence in the results that are used on a daily basis in system validation software suits.

Runtime monitoring & verification of RTES

During the period of the evaluation, several integrated CISTER researchers worked on proposing solutions to develop architectures and frameworks that enable the formal verification of runtime properties of real-time embedded systems. The work resulted in two main contributions: i) a novel architecture for Runtime Monitoring that enforces space and time partitioning between application and monitors, ensuring non-interference between the target application and its monitors [ADAEurope15][RTAS16]; ii) a new framework which includes a formal language for the specification of timed properties to be monitored at runtime and sound and terminating algorithms that allow the synthesis of those specifications into actual code that can be added to the target application in a safe way [RTSS17]. Both i) and ii) have been subjected to real-world applications. The runtime monitoring architecture was implemented in a GNAT/ORK+ Ada runtime system for the space-enabled platforms Leon 2 and 3, and this implementation was successfully integrated in the CONCERTO modelling framework (developed within the European Artemis project CONCERTO). The runtime verification framework was validated in an autopilot control application for commercial UAV, and is a foundational/technological building block in the ongoing ENABLE-S3 and SafeCOP projects, where it is used for requirements specification and the implementation of the demonstrators of three use-cases for different application domains (avionics, automotive, and autonomous agriculture).. These projects involve key international industrial players such as Airbus, AVL, GMV, TTTech, Thales, among others. The software toolbox used in the latter is available online (https://github.com/cistergit/rmtld3synth) and a web interface for specifying and

generating monitors is also available for the community (https://anmaped.github.io/rmtld3synth/), allowing for an easy integration into third-party software developments. The overall work was published in top ranked conferences (RV, Nasa Formal Methods Symposium) in the fields of formal verification and reliable technologies for RTES.

Energy and temperature aware real-time systems

Most of the modern embedded systems are nomadic in nature and hence are battery powered or have limited/intermittent power supply. One of the major challenges in the design process of such systems is to minimise their energy consumption and thus to increase the battery life and enhance their mobility. The current trends in industry indicate: i) an increase in leakage power dissipation, ii) a rise in power density leading to thermal issues that affect the durability and reliability of the hardware platform, iii) a paradigm shift to multicore and manycore hardware platforms design that increases the performance per watt ratio, and finally, iv) an increase in number of I/O devices to facilitate extra functionality. CISTER researchers acknowledged these facts and designed power saving strategies at system-level that mainly target the leakage-power dissipation in modern embedded systems while satisfying temporal constraints of real-time applications. While closing the gap between theory and practice, several prominent energy efficient and cost-effective solutions were designed, receiving over 170 citations. All these results, put together, were disseminated at top ranked real-time conferences [RTAS13, RTNS13, RTCSA13, SIES13, SIES16] and in renowned ISI indexed journals [RTSJ16, JSA16, JSA15, JSA14, MICRO15]. Also, these findings have been implemented and integrated into an open source simulator for power aware and real time systems (SPARTS). Last but not least, this line of CISTER research was exploited in the context of national projects [REGAIN, REPOMUC] and European projects [EMC2, CONCERTO, RECOMP] at various levels of importance, allowing to achieve up to 55% of energy savings and 30% of less pre-emption count on single core platforms, up to 60% of energy savings on homogeneous multicore platforms, and up to 18% of energy savings on heterogeneous multicore platforms. These results are of utmost importance and recognised by the real-time research community.

Advances in wireless communications

CISTER researchers have made a wide range of contributions to the topic of Wireless Communications for RTES over the evaluation period. These successful outcomes culminated in relevant contributions of CISTER to pivotal projects in the area of wireless communications, both national and international, namely: i) in SENODs, the unit contributed to the construction of integrated solutions to address both the cyber and physical challenges posed by the energy consumption, cooling, and operational needs of large-scale datacenters. This effort culminated in 2013/2014 with the production order from PT for hundreds of sensor nodes integrating CISTER solution, and the respective deployment of the sensing infrastructure at PT Datacenter facilities at Covilhã, which had been recently built ground up, to house a state-of-the-art datacenter covering an area of over 12000 m2; ii) CISTER/ISEP acted as leader of the aeronautics domain, chair of the technical board, and member of the strategic board of the DEWI project. CISTER/ISEP also lead the activities of standardization, regulation and certification of the project acting a liaison with the ISO JTC1/WG7 and as leader of the definition of the high level architecture (HLA) of the project. The DEWI HLA is one of the most complete frameworks for the development of interoperable and standardized wireless sensor and actuator dependable networks in industrial applications based on the concept of the DEWI Bubble. The high quality research outcomes of CISTER within these projects can also be witnessed by the participation of the unit as a core partner in follow-up projects: the ECSEL project SafeCOP on safe and secure wireless communications with the objective of evaluating the adequacy and extend current wireless protocols to support safe and secure cooperation scenarios such as vehicle platooning or maritime cooperation actions, and where the unit co-leads a use case on the automotive domain (together with GMV Skysoft); the ECSEL project SCOTT which focuses on high level issues of the Industrial Internet-of-things such as security, privacy, trustiness and safety, and attempts to advance in the

acceptance and trustiness of industrial applications of IoT using a different end-user –oriented perspective of security, privacy and safety issues in industrial applications.

Mobile robots, drones and Robot Operating System (ROS)

CISTER has made several significant contributions to mobile robots and drones system as an example of cyber-physical systems. CISTER researcher, Anis Koubaa, has provided leading works on Robot Operating System (ROS), which is the standard framework for development of robotics applications. He is the Editor of two published volumes of the Springer Book on ROS, and of a third upcoming volume.

A major contribution is the integration of robots/drones into the Internet of Things, in the context of cloud robotics efforts. Research efforts started with the development of ROS Web services, which allowed interaction with ROS-enabled systems through SOAP and REST Web services in a service oriented architecture. The proposed ROSLink protocol enables the access to robots through the Internet via a cloud server. This solution provides an efficient means for a user to access robots without having to deal with NAT translation or hidden domains. Furthermore, the Dronemap Planner (DP) cloud system was developed initially to monitor and control drones over the Internet. It is a cloud-based management system for drones supporting the MAVLink protocol. DP was also extended to support the ROSLink protocol and now enables control and monitoring of any ROS-enabled robot. These contributions were validated with real-world system implementation, and illustrated the Internet-of-Drones/Robots concept. Dronemap Planner is now in the process of commercialization. Current research works focus on safety and security aspects of Internet of Drones.

Vehicular platoons

CISTER also considered a very hot research topic related to vehicular platoons. The main objective is to guarantee the safety of operation of a train of autonomous vehicles in a platoon. This work contributed to outstanding achievements and publications including one US patent, two journal publications and one conference paper. In this research, we designed an accurate simulation model for vehicular platoons using Webot taking into consideration the kinematics and dynamics aspects of the platoon and its physical constraints. We proposed a hybrid controller which is based on two different longitudinal and lateral PID controllers and two operation mode, normal operation mode and degraded operation mode. The normal mode consists in operation without external disturbances and noises that may affect platoon performance. The degraded mode considers external factors that may compromise platoon safe operation, such as degraded communication quality, or noisy sensor data. The safety of platoon was analysed using formal method based on model checking. In addition, we deeply studied the performance of the platoon and reveal its weakness in real scenarios using Webots simulations. The latter includes normal/degraded operating modes, different speeds, full brake scenarios and various Global Positioning System accuracy. Results show the efficiency of the platoon controller even in the pre-defined degraded mode.

Qos in middleware for Cyber-Physical Systems

The abundant research and innovation activities on emerging CPS fields, like IoT, industrial IoT (IIoT), smart grids, smart cities, and similar application areas, have triggered efforts in order to design middleware to support such demanding applications, and later the work was extended to timing aspects and support of QoS requirements on communication middleware and protocols for CPS. In CISTER, this research area has been mostly driven by projects ENCOURAGE, Arrowhead, MANTIS, Productive 4.0. We have contributed to this research field while working on middleware for smart grids (ENCOURAGE project), capable of handling large amounts of data efficiently both in terms of semantic expressivity [TII15] and communication performance [CSI15]. Later on, we have targeted service oriented middleware for industrial CPS (Arrowhead project), where we have led all research activities [ETFA16][WFCS17] regarding expressing, validating and enforcing

Quality of Service requirements. Currently the work developed in Arrowhead is being commercially exploited on a demand-response solution for heat-pumps by NeoGrid, a Danish company. In collaboration with the MANTIS project, also an IIoT middleware capable of collecting information from hundreds of sensors inside industrial machines for Condition-based Maintenance is currently under final tests, for commercial usage. The results are freely available to the public through an Arrowhead framework Wiki. The results in this area are reflected on the publication of 5 book chapters, 10 journal papers and more that 30 conference papers. These achievements allowed CISTER to participate in two ongoing projects that further pursue research on QoS on CPS middlewares for industrial applications (Productive 4.0) and for the automation of power station in smart grids (DSGrid).

Feature extraction in dense sensor networks

The revolution in CPS due to cost-effective devices, allows instrumenting the physical world with high density networks of sensor-rich embedded computation to obtain high resolution sensor readings from the physical world, process it and take better and quicker decisions. To address this area, CISTER has collaborated with CMU, Embraer Portugal and Critical Materials in developing solutions for feature extraction in dense sensor networks. One approach has built upon its research on dominance-based MAC protocols (WiDOM). This work contributed its results to the SmartSkin project for exploitation and resulted in a PhD thesis along with one journal and four conference papers. CISTER is also developing the XDense architecture for complex feature extraction in real-time applications. Using an Aeronautical application scenario, XDense has developed techniques, toolchains and prototype hardware for exploitation as part of both SmartSkin and DEWI projects. This work is supporting a PhD (ongoing), and has resulted in one book chapter, one journal and seven conference papers.

Tech Transfer and Outreach

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During the quinquennium, CISTER participated in many international industry-driven projects (as already reported in Sections “Projects” and “Research Highlights”), with the possibility to exploit and transfer knowledge and technology to industry. Besides these, we would like to stress the number of direct projects funded by industry (Honeywell, Embraer, EFACEC, INOVA+, etc.) and NDA signed.

CISTER has a strategic option of engaging with direct industry funding to develop low TRL projects.

A number of other initiatives were recently launched; these include potential contracts under the K2 Digital Mobility Project (Virtual Vehicle and AVL), Defence offsets in partnership (GMV Portugal and Embraer Brazil) or ESA subcontracts (Thales Edisoft).

Overall, the participation, both in technical work and leadership, has strongly reinforced the role of CISTER as a reference academic institution in the international panorama, which by consequence led to an increase of the requests for the unit to participate in a growing number of new follow-up or novel project proposals, and also to more strategic ventures pivotal to address the societal challenges in domains like automotive (48MEuros K2 Digital Mobility Project approved by the Austrian government, led by Virtual Vehicle) and avionics (Embraer, PhD Program with Austria and GMV).

It is important to mention that in 2016, CISTER started a new initiative, called CiTech, to serve as a formal platform to solidify the national industrial ecosystem working on RTES and to boost the impact of collaborative national R&D in the international panorama. The birth of CiTech was a natural consequence of (i) the successful collaboration record with many national industrial partners and (ii) the international visibility and leadership of CISTER. These national collaborations boosted in 2013 with the CiWork series. CiWork is a 1-day yearly workshop that brings together researchers from CISTER and representatives of major Portuguese companies.

The workshops have adopted two formats, alternating from one year to another. In the first year, companies are invited to expose their latest results and cutting-edge technology, which in turn are used to discuss how CISTER research lines can be adjusted to fit future needs in industry; then the second year, the roles are exchanged. Here, CISTER researchers present a set of fundamental research results and panel discussions with representatives from industry on the potential innovation, benefits, and challenges of applying those results into actual industrial developments.

During the course of this quinquennium, these efforts resulted in more than 30 project collaborations being setup with Portuguese industry for international programs, national programs or direct collaboration. Portuguese companies include GMV Skysoft, Edisoft, Thales Portugal,

EFACEC, Critical Software, Critical Manufacturing, SONAE, Tekever, ISA-Sensing, Embraer Portugal, EVOLEO, Porto Digital, IncreaseTime, Inova+, Portugal Telecom, ADIRA, Virtual Power Solutions and many others. In many of the ongoing international projects, many of these industrial Portuguese players also participate; this is a significant change as compared to previous quinquennia in which Knowledge and Tech Transfer from CISTER was predominantly done only with international industrial players.

During the quinquennium, CISTER researchers have also been actively involved in the discussions related to the Portuguese Government's resolution "Commitment to Knowledge and Science: Commitment to the Future", namely in the thematic of "Cyber-Physical Systems and Advanced Forms of Computation and Communication", being developed by a number of researchers and innovators from academia and industry.

Outreach was also performed by setting-up short-term internships and summer schools (two were organized in 2014 and 2017) to attract younger top students (still in their undergraduate studies), provide them with the core concepts of real-time embedded computing, and challenge them to develop prototype applications.

As already reported, CISTER runs series of internal seminars and distinguished seminars, which are open to the general academic community. In the period of 2013-2017 more than 100 seminars were organized.

Another important vehicle for outreach is the CISTER QuickNews, which is distributed electronically (and also in paper since 2015) to a large list of policy makers, industrialists and academics. The QuickNews is typically bi-monthly; CISTER has distributed and published 37 QuickNews issues during the quinquennium.

Outlook

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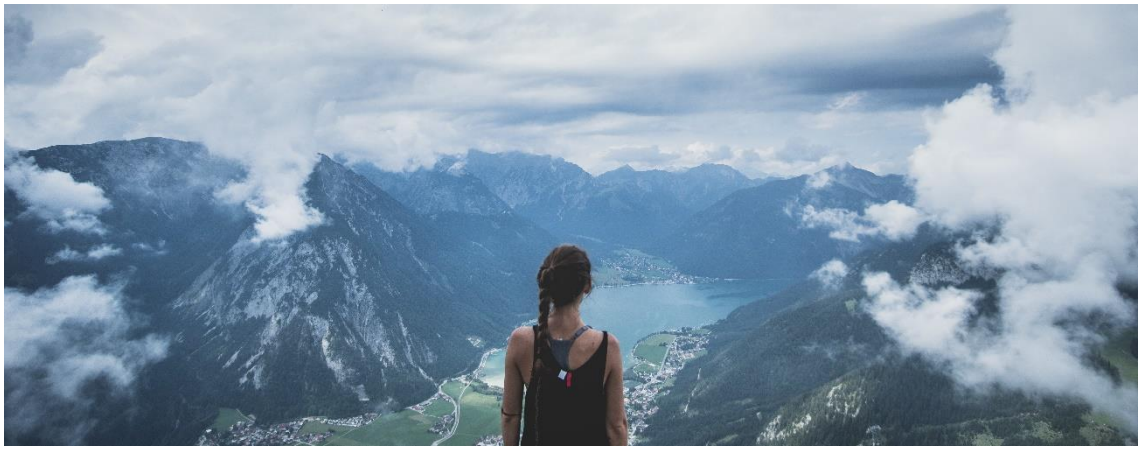

CISTER strategy is built around four main pillars:

1. Sustain an advanced graduation program and create future researchers and domain experts;
2. Produce high quality research with worldwide visibility and recognition;
3. Create strong national and international networks to exchange knowledge, promote and improve the quality and reach of embedded systems research in Portugal and internationally;
4. Enable successful technology transfer towards industry.

To sustain this program, we consider that the following actions must be implemented during the period 2018-2022.

PhD students

During the quinquennium 2013-2017, CISTER had around 23 PhD students active every year. This number fell slightly in the last three years, to 20 active PhD students in 2017. As already explained, our impediment to grow the number of students during the last 5 years was due to a combination of factors, two of which were out of the unit's control (i.e., cost of tuition fees for PhD students doubled and FCT PhD-student scholarships – which are the only ones to cover tuition – became more difficult to non-EU citizens).

For the coming quinquennium, CISTER plans to increase the number of PhD students to around 30-35 at the end of the period (i.e., an increase of 50% as compared to the number at the end of 2017). Our goal is to reach an average of 2 PhD students per integrated PhD member and an average of 3 PhD students per FTE at the end of 2022. To this end, we plan to enrol around 14 new PhD students already in the biennium 2017-2018 (4 of which are already enrolled as active at the end of 2017), and to attract around 6 to 7 new high-quality PhD students every subsequent year. With an expected number of 4 graduations per year on average (similar to the last quinquennium), this would let us reach the target of 30 to 35 active PhD students in 2022.

To support these new engagements, CISTER is planning an average of 3 new PhD-student grants per year paid by FCT via part of its pluriannual funding (programmatic funding). The other PhD students will be financed in part by national projects or other types of FCT grants obtained through competitive calls, and in part by European projects and direct industrial funding. In these cases, the tuition fees will be paid with projects' overheads or will be covered by the industrial collaborators. It is important to note, as already explained, that for the coming quinquennium there will be more availability of the overheads to pay tuition fees, as one of the main consumers of overheads during quinquennium 2013-2017 (cost of building use) ended in 2016.

Integrated PhD members

As mentioned earlier in this report, the number of currently integrated PhD members is 16. 8 of those members account for only around 25% of the FTE integrated PhD researchers, because they have important teaching (and some cases, RTD management) duties.

Most of the other 8 members are essentially full-time researchers. However, despite being with CISTER for more than 3 years (6 years in some cases) those 8 PhD members are supported by grants of typically 6 months or 1 year duration; those grants are funded out of projects or out of the unit's pluriannual funding. The lack of stability of those researchers hinders better long term-planning that could enable the research unit to better compete for external funding, and to coordinate and supervise a larger number of research activities (including PhD students). In addition, it is not optimal with respect to the ambitious agenda of the research unit related to transfer knowledge and technology, and engagement with industry-driven low TRL collaborations.

The application of the recently adopted Portuguese law (Law 57/2017), and specifically Article 23 in that law, will significantly mitigate the current issue of having full-time researchers for long periods based on a sequence of short-term grant-based contracts. With the application of the new law, a process is already started via which the unit can offer an equivalent number of longer-term contracts (typically 6 years) or tenured contracts, for which FCT will provide significant financial support. The research unit policy will be to have all full-time PhD researchers (apart from typical postdoc cases) based on longer-term contracts which are now enabled by the new legal framing.

By implementing this action, it will be possible for CISTER: (i) to build a more stable long-term research strategy supported by permanent full-time researchers; (ii) to ensure increased stability and commitment of those researchers towards directing PhD students; and (iii) to boost the capability to engage in even more research projects (international, national or direct industry-funded), where those full-time researchers can act as Principal Investigators.

The opportunity offered by the new law (Law 57/2017), and the commitment by both FCT and hosting institutions to provide the financial instruments to support its implementation, allow CISTER to strategically direct the request for pluriannual FCT programmatic funding to direct grants for PhD students and towards participation in initiatives such as the Air-Centre initiative.

Compelling set of World-class Research Topics

Along with their pervasiveness and ubiquitous deployment, embedded platforms are becoming increasingly complex as they grow more powerful and heterogeneous, owing to ever increasing and demanding requirements, as well as specialization for demanding features. Their complexity and resource-awareness brings further challenges to the development of reliable, efficient and time-predictable systems. In fact, the embedded computing field is nowadays one of the fastest evolving one, with limits being pushed every day. This arises from new disruptive applications such as the internet of things, smart factories or autonomous vehicles. Autonomous high-performance applications are required to safely operate in complex heterogeneous systems, ranging from entirely centralized to highly distributed systems, and integrating simple hardware with limited power, memory and computing capabilities together with platforms including multi and many-core processors, GPUs, and FPGA accelerators.

It is therefore understandable that CISTER's activity plan for the forthcoming years aligns with the international R&I agendas and societal challenges (e.g., H2020 advanced computing and CPS, ECSEL MASRIA, ITEA living roadmap), and in particular in research directions which build upon the centre's internationally recognized topics.

As noted before, the main focus of the centre's activities is on the impact of the non-functional timing properties of embedded systems in its correct functioning. This implies ensuring the systems' safety and dependability through both novel timing and schedulability analysis methods, which are able to reason on the temporal behaviour of the system and detect abnormal behaviour,

enforcement of timing properties, through novel or extensions to existing programming and specification languages, OS mechanisms, communication protocols, middlewares, and reference architectures for the development of the next generation of real-time embedded systems. As already stressed in prior sections (Projects and Research Highlights), CISTER has a successful track record in these topics, applying its research results to various domains such as automotive, avionics, space, railway, smart buildings and factory automation, in which timing properties play a crucial role.

Taking into consideration the new existent challenges, and the solid background developed at CISTER, the centre's roadmap includes development of world-class research in:

- analysis and algorithms to enable safe timing execution of high-performance real-time applications on complex heterogeneous platforms, including multi and many-core platforms, GP-GPUs and FPGA accelerators;
- analysis and communication mechanisms for dense and highly connected sensor and actuator systems, able to provide timely information and control, even with complex topologies, based upon latencies and timelines as structuring concerns;
- time and space isolation mechanisms for safety-critical and mixed-critical systems, build on top of complex embedded computing platforms (multi-core and many-core);
- interplay and dependencies between time and other non-functional properties such as energy, reliability and security, as more and more solutions need to devise an "optimal" operating point with several competing requirements;
- methodologies and algorithms to enable analysis and configuration from model-based specification of systems, and systems of systems, thus enabling validation of timing properties to be performed early in the development process, considering multiple stakeholders;
- methodologies and algorithms to enable to formally monitor timing behaviour and adapt to changing operation conditions;
- methodologies and mechanisms for incorporating quality of service and service level agreements as a structural component at all layers of complex cyber-physical systems and internet of things frameworks;
- analysis of safety and security of drones over the Internet and design of appropriate approaches to ensure their functional safety;
- contribute to the integration of robots and drones to the Internet of Things and cloud with satisfaction of real-time constraints and quality of services;
- contribute to the development of innovative solutions with Robot Operating System (ROS) and its integration into cyber-physical systems.

These topics are already being addressed (in different stages), both in more fundamental research works (in the past funded by FCT projects) and PhD studies, to more applied industry-driven research particularly in large European projects.

Publications

As discussed in the Publications section of this report, CISTER published, per FTE in the quinquennium 2013-2017, an average of 8.7 indexed journals, 1.6 top-core conference papers and 7.1 other-core conference papers. Although those numbers are appreciable, CISTER will aim at increasing the number of publications in top-core RTES conferences during the next 5 years. This will be supported by the increase and renovation of the PhD-students pipeline, as well as by the improved stability offered by the longer-term contracts for the full-time PhD integrated researchers.

Projects

Fundamental research projects funding is important to CISTER's strategy as it typically allows for supporting a fraction of the PhD-students (those not directly funded by PhD-student FCT grants) and it is crucial to enhance the creation of competitive knowledge and competencies. As it was mentioned earlier in this report, one of the main sources for that type of funding used to be FCT-funded projects. Unfortunately, during the quinquennium 2013-2017, FCT had only two full-fledged calls launched; the 2014 call and the 2017 call (for which results are not yet known). This was a different situation as compared to the previous quinquennia. It is worth mentioning that in quinquennium 2008-2012, during which FCT-calls for projects existed every year, CISTER was able to win 12 new proposals (2-3 per year) in calls launched in the 2008–2012 period.

CISTER had typically an acceptance rate of 40%, during the quinquennium 2008-2012, which was well above the average acceptance rate (typically 15%) in those calls. Considering the plans of FCT to reinstall the yearly project calls, it is expected and credible that CISTER will be able to steadily increase the number of active FCT fundamental-research projects to reach by 2022 the number shown for the early years of quinquennium 2013-2017 (around 11-12 active projects).

CISTER is also engaging with a larger set of instruments that will enable other sources of funding, including funding to support PhD-students. There is a growing number of direct-industry collaborations for developing low TRL efforts. These include companies such as Embraer, EFACEC, Honeywell or Critical Software, with new contracts already in place for 2018. Furthermore, CISTER is exploiting with collaborations with companies for defence offsets funding (one proposal submitted in December 2017 and being evaluated) or the participation of CISTER in large strategic projects/programmes such as is the case of the 2018-2022 COMET K2 Digital Mobility 48MEuros programme being managed by Austrian key players; this initiative has tens of industrial players from Europe offering a new set of initiatives and synergies that CISTER will be able to exploit in conjunction with the H2020 calls or even directly with funding from the COMET K2 initiative itself.

It is important to mention the current strategic European programs in the area of embedded systems and cyber-physical systems such as ECSEL or ITEA. CISTER researchers are very active within those two programmes, and in the past quinquennium, CISTER successfully engaged and participated (with multiple leading roles) in numerous of the funded international projects. In the past 2 years, the level of financial commitment of the Portuguese authorities in those programs (which have national co-funding) was reduced by economic reasons, and therefore this already affected slightly CISTER e.g., in the ECSEL 2017 call for projects. CISTER was in the front-row, in association with a number of other national industrial key players to mitigate that problem and a new funding instrument was made available (through Portuguese Innovation Agency – ANI) to support the participation of Portuguese players in those strategic international programs. CISTER will again, in 2018, focus on ECSEL project opportunities, in parallel with other H2020 calls.

CISTER has been an active member of various national clusters since a number of years; notably, PEMAS (Portuguese Industry Aeronautics Association) and AED (Aeronautics, Space and Defence cluster) and collaborations with companies involved have been growing significantly in articulation with the instruments that CISTER is nurturing; namely the CiTech and CiWork initiatives. It is more than expected that funding coming from direct industry contracts will keep growing steeply.

It is also worth to mention the continuous effort CISTER is doing in adapting the core research competences to cover a growing number of application domains. Two examples worth to mention are (i) the interplay between security and safety and (ii) the integration of artificial intelligence technologies in real-time embedded systems. Concerning the former, a larger structured collaboration is being developed with Altran Portugal to be materialized soon.

Knowledge transfer, technology transfer and Outreach

The activity plan of CISTER foresees to continue and reinforce transferring knowledge and technology between the unit and industry. It will do so through both industry-driven projects and direct subcontracting with companies. The latter case will be in particular reinforced; the unit plans to formally create a tech transfer office, in articulation with companies, an initiative which has already been presented and informally named CiTech.

In this scope, and to further solidify its close connection with industry, CISTER will continue to organize a yearly workshop (CiWork) that brings together researchers and practitioners from the industry and academia and provides them with a bidirectional platform to report and discuss on the recent advances and developments in the area, as well as current and potential solutions for industrial applications.

In parallel, the unit will work with the hosting institutions to promote IPR policies, balancing the needs of industrial collaboration with the capacity of publishing results in scientific conferences and journals. CISTER is a research centre, and collaboration with industry should not impact the ability of its students and researchers to openly publicize their results.

CISTER will proceed implementing its CISTER QuickNews well-succeeded dissemination and awareness effort. The CISTER QuickNews is distributed bi-monthly to policy-makers, industrialists and members of the society.

SWOT

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S	**STRENGTHS** • Recognition & leadership • Strong international network • Capability of attracting competitive funding • International working environment • Facilities	INTERNAL	**W** **WEAKNESSES** • Hard to compete at the international level w.r.t. salary levels • Permanent members cannot devote more than 50% of time to RTD, including management, because of high teaching loads
HELPFUL			HARMFUL
O	**OPPORTUNITIES** • Growing importance of RTES • Porto is a new International tech hub in safety-critical computing • Enlarging the institutional commitment (ISEP + FEUP) • The stability that will be provided by new contracts (law 57/2017) to a few CISTER PhD researchers • Reduction of tuition fees for PhD students from 2017-2018	EXTERNAL	**T** **THREATS** • Talent Acquisition & Retainment • Funding sources; specially for fundamental research projects (e.g., the national research council was not opening enough calls during the last quinquennium)

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