

# A Multicore Processor Platform for energy and throughput aware application

Ishfaq Hussain, Yasir Qadri, Ayaz Ahmed, Nadia N. Qadri  
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# Sequence Of Presentation

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- ❑ Need For Energy Optimization
- ❑ Problem Statement
- ❑ Proposed Solution
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- ❑ Conclusion
- ❑ Research Contribution
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# Introduction

- The project “A Multicore Reconfigurable Processor Platform for Energy and Throughput Aware Applications”.



# Project Team Overview

- Members were divided into two groups
  - Hardware Development
  - Algorithms Development.
- Each group worked on their team specific issues.

# Need For Energy Efficient

Energy Efficient system design is important due to following reasons

- Portable Devices
  - ✓ Examples: Mobile Phones, PDA, Laptop
- High-end Desktop/Server Computing
- Green Computing

# Technique to reduce Energy consumption

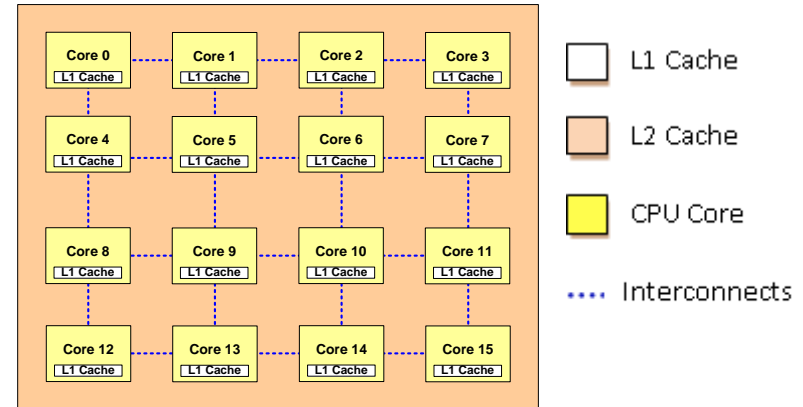
- Logic level
  - Clock Gating
  - Power Gating
- Micro-architectural level
  - Cache memories
  - Pipelining
  - Buses
- System level
  - Dynamic Voltage-Frequency Scaling (DVFS)
  - Adding Parallelism
  - Reconfiguration

# Reconfigurable Architecture

- Contemporary Processor Architectures
  - ✓ Designed for overall average performance
  - ✓ Do not leverage much flexibility for reconfiguration
  - ✓ Limited application of Energy aware throughput management
- Reconfigurable Processors
  - ✓ A recent contender for energy/performance
  - ✓ Need to go beyond traditional DFS and Core switching approach

# The System Architecture

- ❑ A multicore architecture with an Artificial Intelligence algorithm based reconfiguration engine
- ❑ Input Parameters
  - ✓ Energy Consumption
  - ✓ Throughput
  - ✓ Miss Rate
- ❑ Reconfigurable Parameters
  - ✓ Number of Cores
  - ✓ Operating Frequency/Voltage
  - ✓ L1/L2 Cache Size
  - ✓ L1/L2 Cache Associativity



Parameter	Value
Processor Type	Intel x86
Number of Cores	16
Operating Frequencies	[16, 20, 25, 33] MHz
Operating Voltages	[2, 2.2, 2.4, 2.7]V
Energy Consumption per cycle	[13.1,15.4,18.7,22.9]nJ



# Optimization Algorithm

- **Fuzzy Logic Type 1**
  - **Mamdani**
  - **Sugeno**
- **Fuzzy Logic Type 2**
- **Ant Colony Optimization**
- **Genetic Algorithm**
- **Estimation of Distribution Algorithm**

# Comparison with state of the art

Parameter/ Architecture	Intel IA-7	NVIDIA	RENT Cache1	RHC 2	RAMPSoC3	ACODSEE
DFS	Y	N	N	N	Y	Y
Core Switching	Y	N	N	N	Y	Y
Cache Associativity	N	N	Y	Y	N	Y
Cache Resizing	N	Y	Y	Y	N	Y
Energy Efficiency Scheme	Proprietary	None	None	None	None	ACO

RENT: Reconfigurable Energy Efficient Near Threshold Cache Architectures

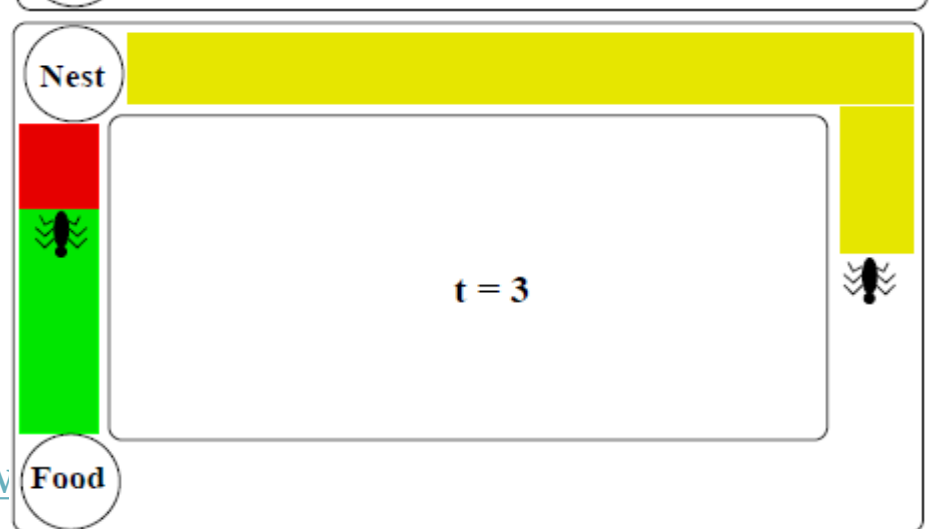
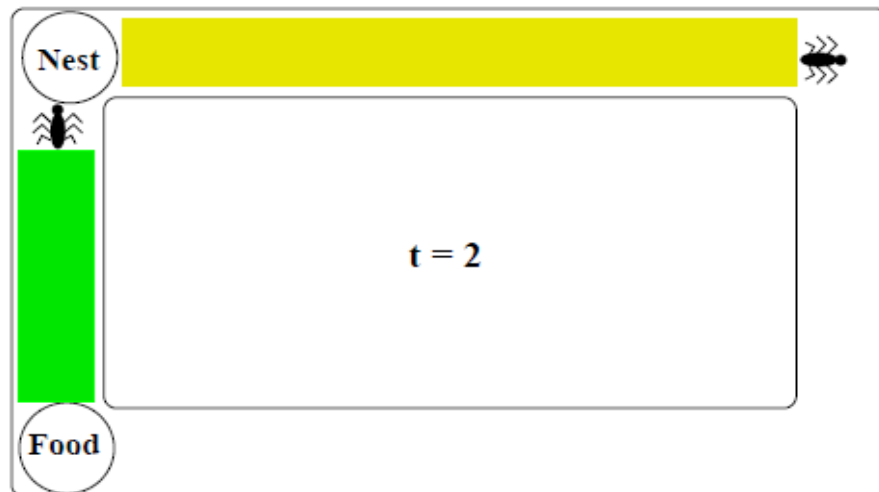
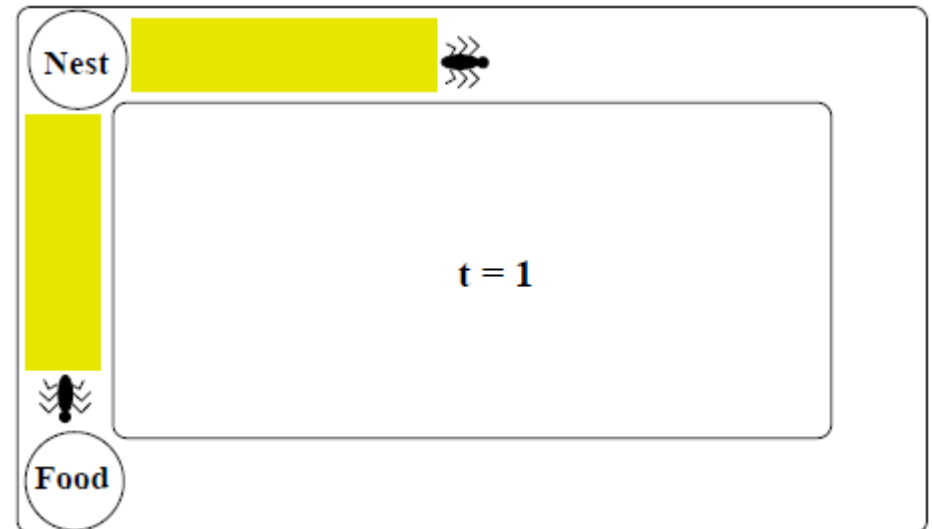
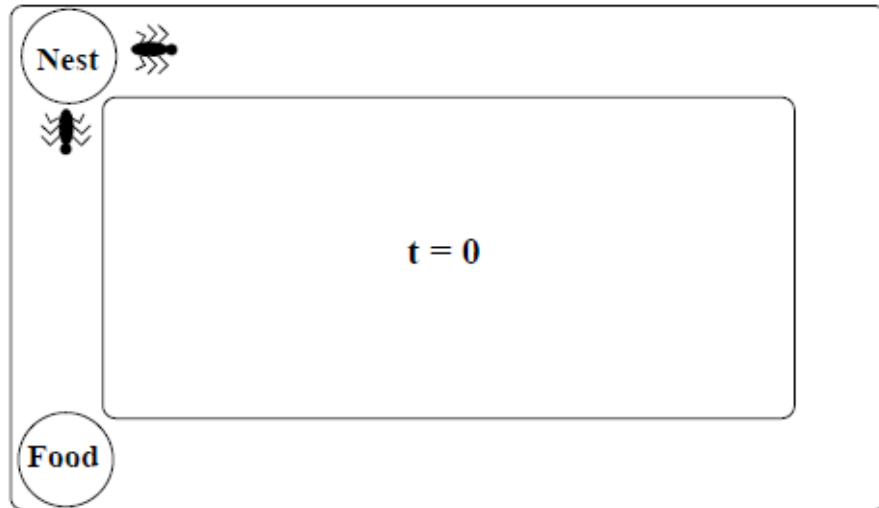
RHC: Dynamically Reconfigurable Hybrid Cache

RAMPSoC: Runtime adaptive multi-processor system-on-chip

ACODSEE: Ant colony optimization based design space exploration engine

# Reconfiguration Engine

# What is ACO ?



# Continue..

- Probabilistic Selection

$$p_c(u/q) = \begin{cases} \frac{[\tau_{qu}(t)]^\alpha [\eta_{qu}]^\beta}{\sum_{k \in \text{allowed}_k} [\tau_{qu}(t)]^\alpha [\eta_{qu}]^\beta} & \text{if } j \in \text{allowed}_k \\ 0 & \text{otherwise} \end{cases}$$

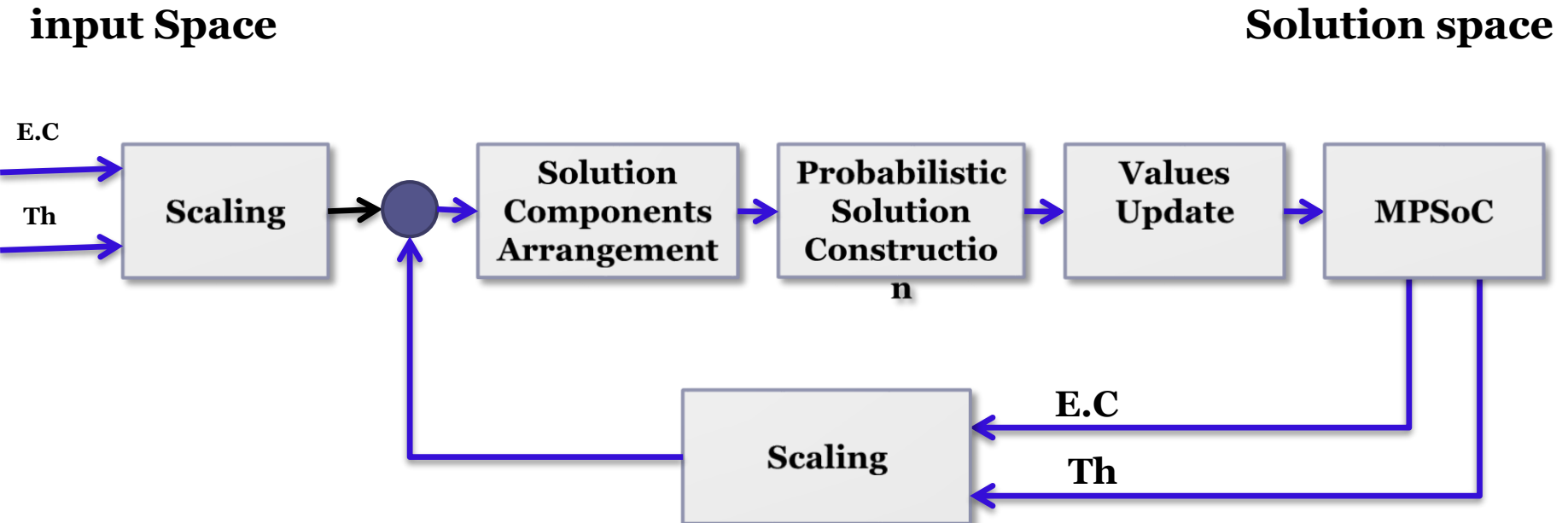
## Global Pheromone Update

$$\Delta \tau_{qu}^{\text{Global}} = \begin{cases} \frac{Q}{e_{\text{best}}} & \text{iff } (qu) \in \text{bestTour} \\ 0 & \text{otherwise} \end{cases}$$

- Pheromone Update

$$\tau_{qu}(k+1) = (1-\rho)\tau_{qu} + \Delta \tau_{qu}^{\text{Local}} + \Delta \tau_{qu}^{\text{Global}}$$

# Exploration Engine



**E.C → Energy Consumption**  
**Th → Throughput**

# Experimental Platform

# Simulation setup

Basic modules of the simulation scheme are

- **Exploration Tools**
  - ✓ **MATLAB**
  - ✓ **M3 Explorer**
- **Simulation Setup**
  - ✓ **MARSSx86**
  - ✓ **SESC Simulator**
  - ✓ **Ubuntu 12.04**
  - ✓ **SPLASH-2**
  - ✓ **CACTI**
  - ✓ **Mathematical Model [7]**



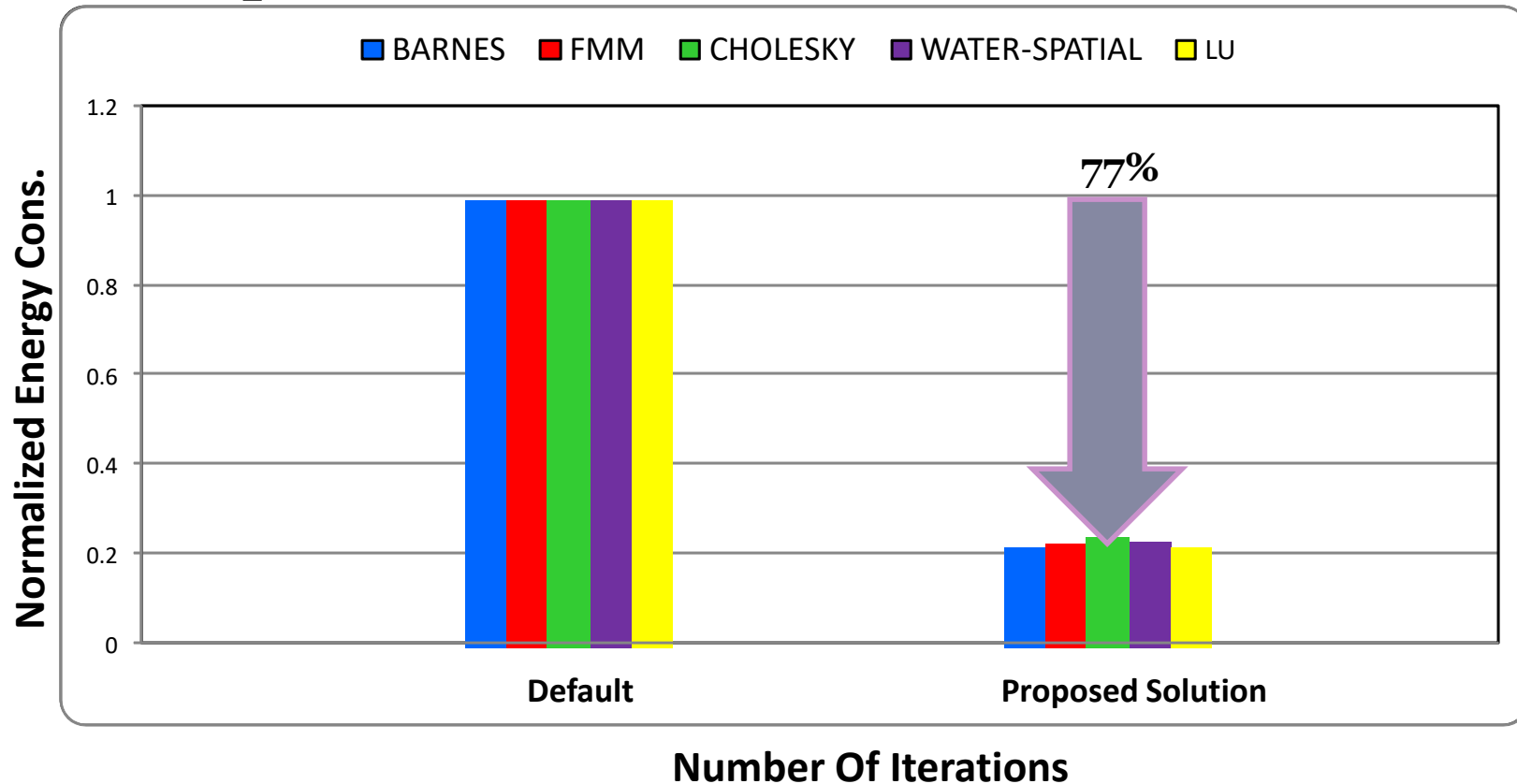
# Results and Analysis

# Results

Iterations	Cores	Operating Frequency(MHz)	L1 Cache Size (Kbytes)	Normalized Energy Consumption	Normalized Throughput
Default	16	33	256	1.00	1.00
1	4	25	128	0.31	0.7172
3	9	25	8	0.51	0.64727
5	11	25	16	0.55	0.72618
7	3	33	64	0.23	0.93173

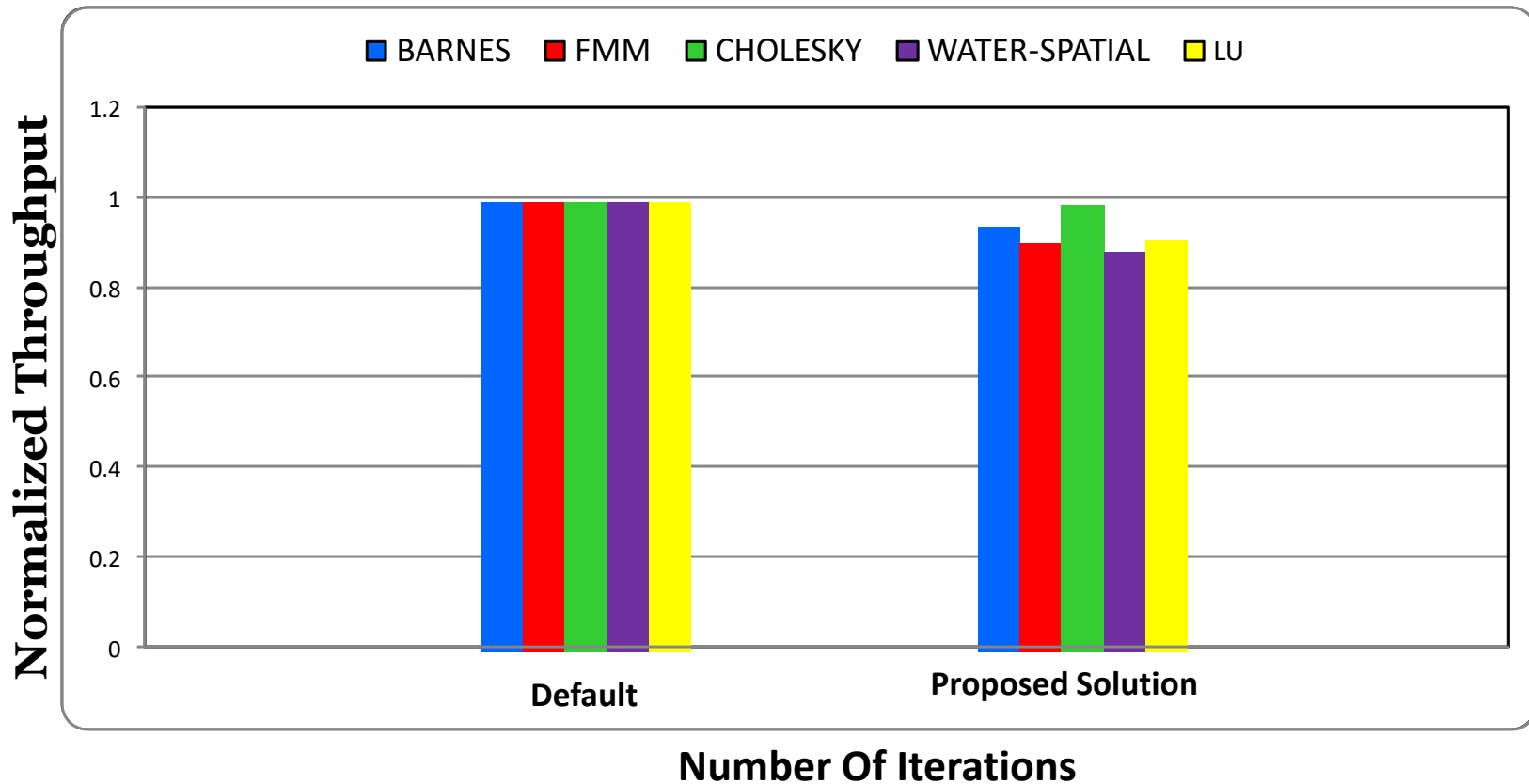
# Results

## Impact of ACO based DSE engine on normalized energy consumption



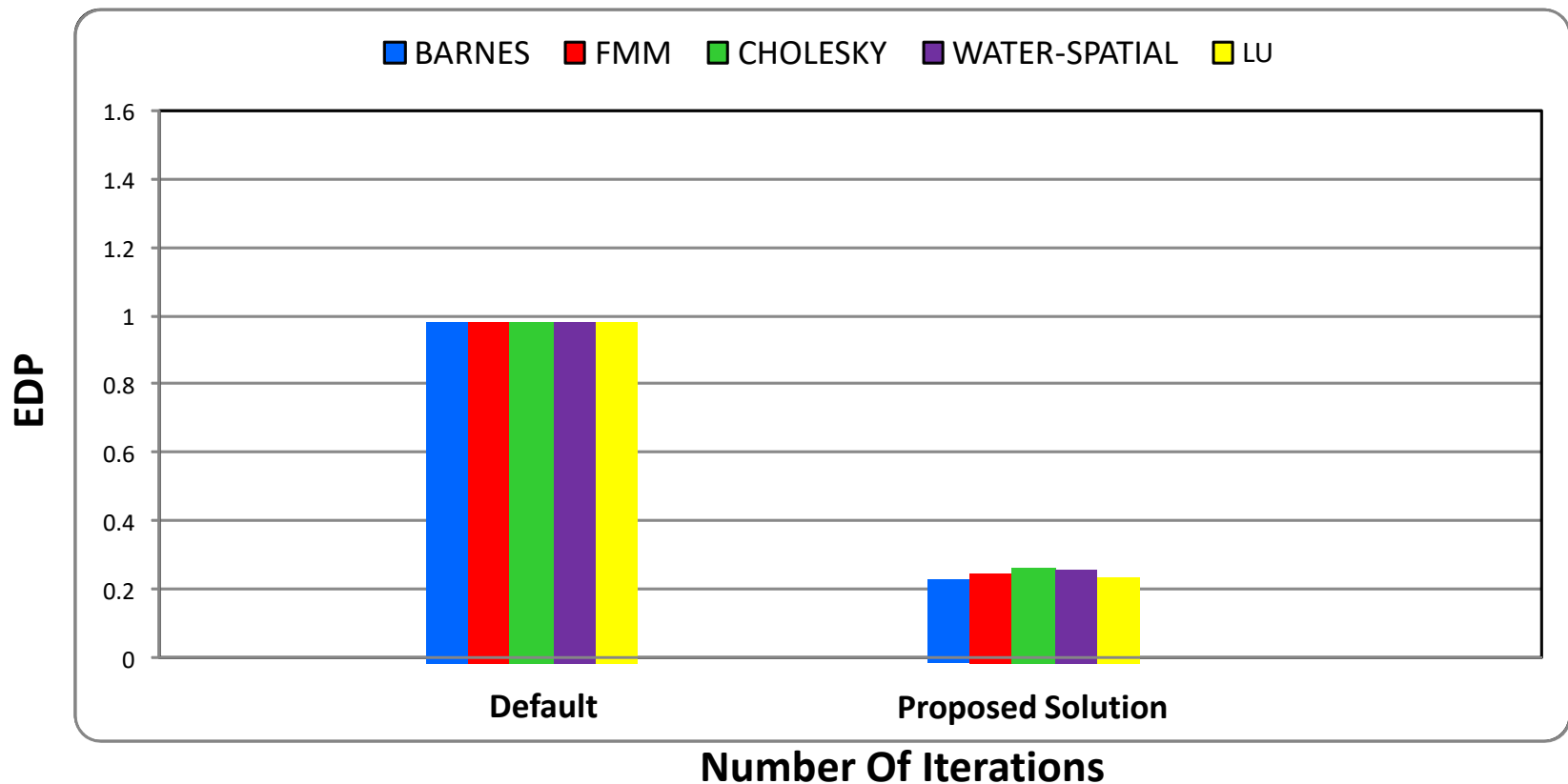
# Results

## Impact of ACO based DSE engine on normalized throughput



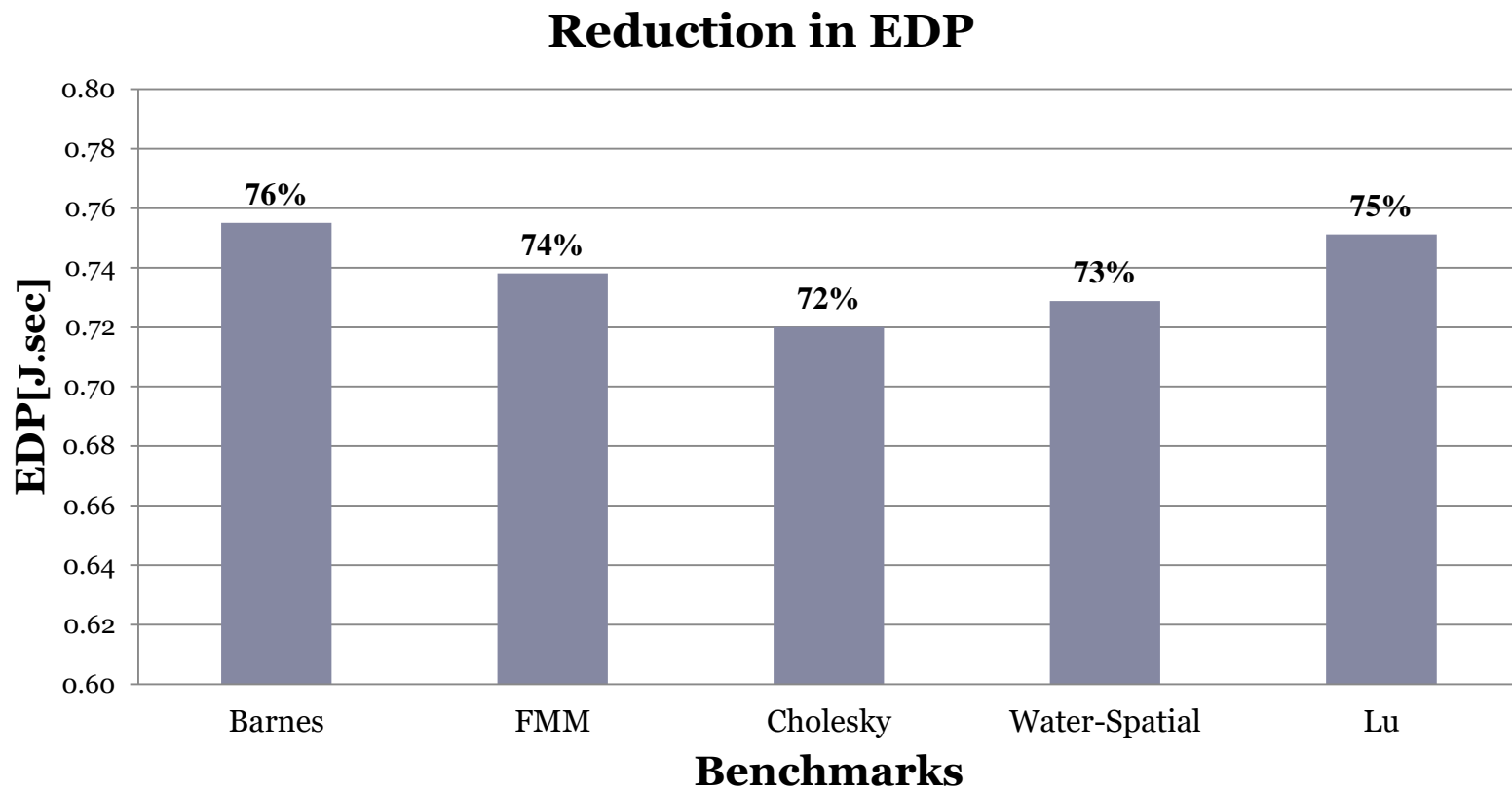
# Results

## Impact of ACO based DSE engine on EDP



# Results

Average reduction in energy delay product (EDP) of all Benchmarks



# Conclusion

- The design space explored by ACO is validated using various SPLASH-2 benchmarks, and simulation results reveal that on average, 77% energy consumption is reduced at the cost of only 7% reduction in throughput
- Therefore it can be concluded that the proposed ACODSEE successfully propose energy and throughput efficient solution for a Multicore architecture

# Research Contribution

- Hussain, Ishfaq, et al. "Ant Colony Optimization for multicore re-configurable architecture." *AI Communications* 29.5 (2016): 595-606.
- Hussain, Ishfaq, et al. "NSGA-II-Based Design Space Exploration for Energy and Throughput Aware Multicore Architectures." *Cybernetics and Systems* 48.6-7 (2017): 536-550.



# Thank you

# Questions?