

Mixed Criticality Scheduling with Memory Regulation



CISTER - Research Centre in Real-Time & Embedded Computing Systems

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Motivation

- A trend towards running different mixed-criticality applications on a single core.
- Mixed-criticality systems require certification.

Issue

COTs multicore platforms have contention over shared resources

- Hard to analyze WCET of a task due to low predictability. This leads towards pessimistic bounds for WCET, resulting in low resource utilization.

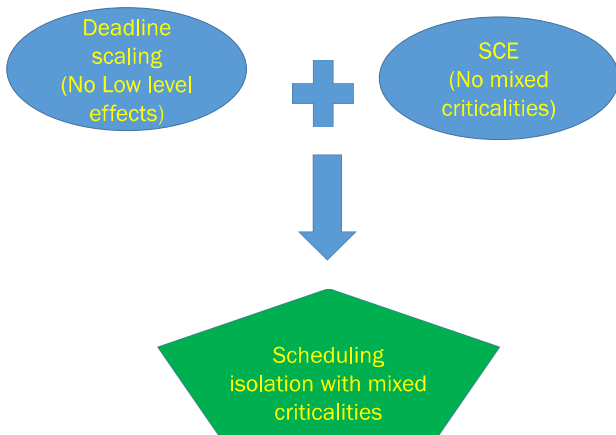
Proposed Approach

Memory regulation technique (Single Core Equivalence - SCE) is adapted. This approach did not explicitly consider mixed criticalities until now.

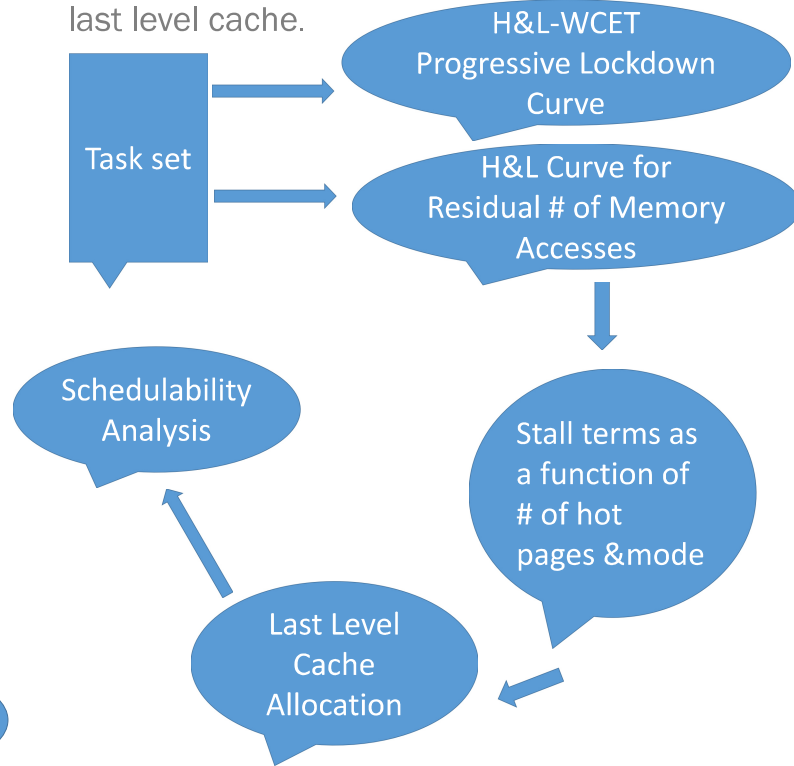


Contribution

- Vestal's based L-WCET and H-WCET for 2 level criticality tasks in 2 modes(L and H).
- Ekberg and Yi's deadline scaling technique extended by incorporating the effects of contention under SCE's memory regulation scheme.



- Progressive lockdown curve: WCET in isolation as a function of # of hot pages in last level cache.



What more!

After the mode change, L-tasks are dropped. Thus the resources allocated to them (like cache partitions) are idle

Idea

Utilize the L-tasks' resources for the available H-tasks. Based on Integer Linear Programming (ILP) model taking into account the # pages in the last level cache for both modes, and resource utilization)

Future Work

- Design of simulator for the implementation of proposed work.
- Implementation of dbf-based schedulability tests.

References

- S. Vestal, "Preemptive scheduling of multi-criticality systems with varying degrees of execution time assurance," in 28th RTSS, 2007.
- P. Ekberg and W. Yi, "Bounding and shaping the demand of mixed-criticality sporadic tasks," in 24th ECRTS, July 2012, pp. 135-144.
- R. Mancuso, R. Pellizzoni, M. Caccamo, L. Sha, and H. Yun, "WCET(m) estimation in multi-core systems ECRTS, July 2015, pp. 174-183.